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Single Port TDR Test For Calibrated S-Parameters

James Mayrand, Complete DVT Solutions
274 Piper Road, PO Box 291
Ashby, Massachusetts 01431
URL: www.cdvts.com
Email: mayrand@earthlink.net
Phone: 415-738-8607

Brian Shumaker, Complete DVT Solutions
1011 Riverton Drive
San Mateo, CA 94070
URL: www.gigaprobes.com
Email: b.shumaker@comcast.com
Phone: 650-593-7083

Abstract

This paper describes a unique one port TDR test technique on an IP transceiver network characterizing performance by extracting two port S-parameters. Because of the lack of access at the system level, a one port measurement is essential. This is a typical VNA measurement but because of the lack of access, a TDR test is essential for this full S-parameters characterization. The technique allows for extraction of accurate S-parameters for Spice modeling, eye pattern generation and Impedance profiles for determining min and maximum interconnect performance. This paper describes using this technique to characterize a 10 Gigabit transceiver interconnect network performance and the steps required for generating a two port accurate S-parameter from a one port TDR measurement. The results obtained includes device effects such as package balls and corresponding ball pads. This could be essential for characterizing lead free solder failures at the system level.

Author(s) Biography

Jim Mayrand -Dir. Engineering for Complete DVT Solutions. Has a Masters of Science Degree in Electrical Engineering, serves as the senior advisor to UNH Inter-operability laboratory used to define and implement Gigabit Test Standards. Has extensive backplane and ASIC design experience with in-depth knowledge of both interconnect and IC device physics up to 40Gbit. He retired from Hewlett Packard as a hardware design engineer, he worked in the semiconductor product test and design engineering field and holds five Patents. Has been an on site trainer and software application developer for Tektronix's SI software IConnect/MeasureXtractor for 5 years.

Brian Shumaker Dir. Sales and Marketing for Complete DVT Solutions. Has 35 years experience in sales and marketing test and measurement instrumentation. 14 years at Tektronix; 4 years as a VLSI and High Speed Digital accusation system specialist; 11 years Test and Measurement Tektronix sales. As an independent contractor, worked with companies to define and bring their product to market including a line of Robotic probing and manual Signal Integrity probe stations. He worked for TDA Systems 4 years selling and marketing Signal Integrity IConnect/Measurement Extractor software, now a Tektronix product.

INTRODUCTION

Using this analysis technique makes it is easy to extract S-parameters, eye diagram, impedance profiles and Spice models. Time and frequency test data failures can quickly isolate the failing component. This can be done by analyzing eye diagrams and impedance profiles. If the network S-parameters are not within acceptable limits, it can be quickly determined whether the failure is the IC or the printed circuit board. This analysis creates an opportunity to balance IC and PCB RF performance to minimize repair costs and cycle time. The measurement based Spice models can be used by the design engineer to make the necessary interconnect speed enhancements.

Test Case

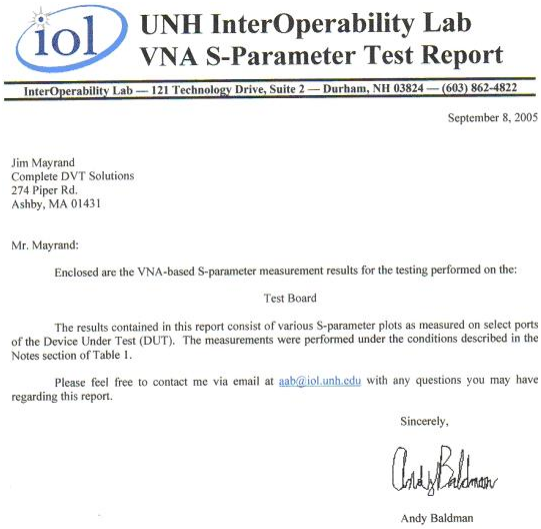
As an example, a USB device test board and IC package was failing return loss (S11<-10dB). To debug the problem, the customer wanted to measure both insertion and return loss but the IC terminator was 50 ohms but could not be accessed. For this case a TDR test could only be used and no TDT measurement could be accessed. The second port TDT was extracted from the reflected wave to generate two port S-parameters and this method of TDT extraction will be described in this paper. To identify the cause of the S-parameter failure, we used IConnect® and advanced HSpice techniques to analyze the USB interconnect components in the time domain which would identify the faulty device. Key to this test plan was that we did not want to redesign expensive components such as the transceiver IC but rather change the board or its components. To save costs, we studied a variety of printed circuit board enhancements to improve test margin. Then we let the customer decide which changes to make.

Test and Modeling Steps for Extracting Two Port S-parameters:

1. Calibrate TDR to VNA data from a Golden Test Board
2. Standards for calibrating TDR and VNA instruments
3. Conditions for one port TDR measurement
4. Open TDR measurement using differential GigaProbes™
5. Partition open TDR to extract RLGC component information
6. Optimize Hspice model to emulate TDR using IConnect®
7. Simulate TDT in Hspice
8. With Simulations, generate Eye Pattern and S-parameters
9. Differentiate the failure using Eye diagram or S-parameters

Calibrate TDR to VNA data from Golden Test Board

A third party VNA correlation standard methodology is required to resolve routine conflicts between VNA and TDR S-parameters so its recommended that a 3rd party be used such the University of New Hampshire Interoperability Laboratory (UNH) (http://www.iol.unh.edu/) or a local metric lab where an independent compliance engineer conducts VNA tests to correlate and validate our TDR measurements. In this case, the VNA hardware configuration used at UNH was an Agilent VNA Model N1951A 20GHz PLTS to extract the s-parameters from 6 inches of etch on a SMA terminated IP test board. Attached is an example of a Certificate of Compliance proving the measurements were tested by an independent test lab for Complete DVT Solutions. It is recommended that the **same standards be used to calibrate both TDR and VNA instruments.** Additionally, both instruments must use the similar frequency range and calibration procedures.



UNH InterOperability Lab
VNA S-Parameter Test Report

InterOperability Lab — 121 Technology Drive, Suite 2 — Durham, NH 03824 — (603) 862-4822

September 8, 2005

Jim Mayrand
Complete DVT Solutions
274 Piper Rd.
Ashby, MA 01431

Mr. Mayrand:

Enclosed are the VNA-based S-parameter measurement results for the testing performed on the:

Test Board

The results contained in this report consist of various S-parameter plots as measured on select ports of the Device Under Test (DUT). The measurements were performed under the conditions described in the Notes section of Table 1.

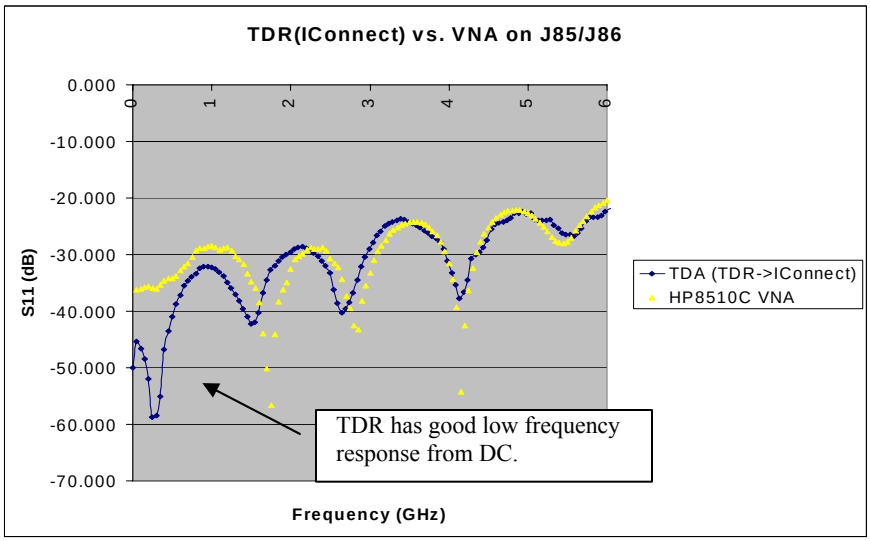
Please feel free to contact me via email at aab@iol.unh.edu with any questions you may have regarding this report.

Sincerely,

Andy Baldman

6 GHz TDR to VNA Calibration Test Example

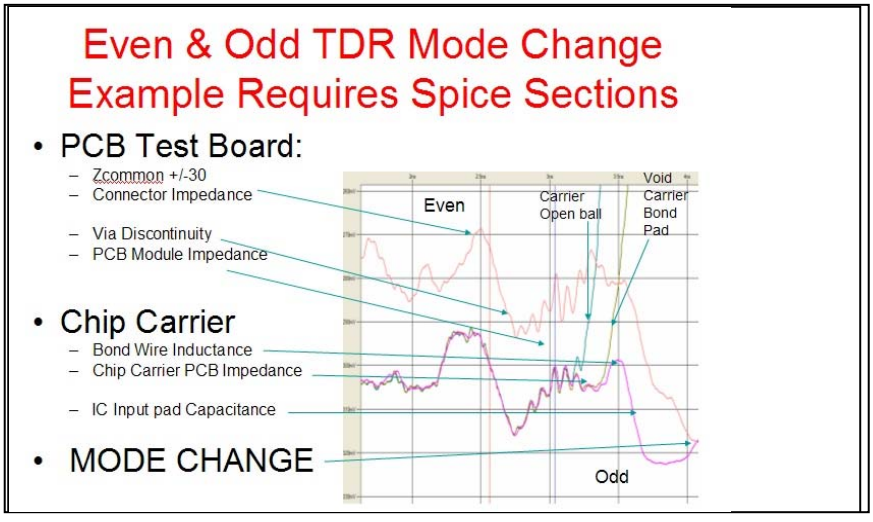
a 50 ohm calibration S-parameters were generated from TDR and imported into an Excel spreadsheet along with the VNA data from UNH. When porting VNA to Excel for correlation to IConnect®, it was found that a 20 GHz Agilent VNA generated SnP files when transformed to the time domain, only supported edge rates > 60ps. Whereas a 30ps TDR was found to accurately model system edge rates below 50ps but it start at DC. The VNA start frequency was 50MHz instead of the preferred start frequency of 300 KHz as demonstrate by the spreadsheet graph below. Another correlation issue is time domain record length. The Tektronix TDR had 4000 time points vs Agilent of 1500 frequency points. No matter which instrument you use the resultant SnP file imported into Hspice as a behavioral model must have the same number of points and start frequency must be the same. For maximum TDR bandwidth, measurements should be taken with sampling head extenders and short matched test cables to the Device Under Test (DUT).



TDR versus VNA showing DC correlation errors

Hybrid Models for Open TDR measurements

Regardless of how you test networks, IConnect® partitions or "time gates" the measurements into accurate differential W models. IConnect® can "automatically determine" when interconnect changes Mode and can model TDR measurements. The graphic below is the result of IConnect's topological modeling process using multiple TDR measurements to define the end of physical sections (i.e. ball, chip carrier) IConnect® produces a "measurement based" topological model that allow sections to be saved as a primitive model (i.e. via) and recompiled into new design architectures. They can be compiled into hybrid models containing topological and behavioral models. These models are polymorphic; meaning they can be re-reused to meet many new applications without returning to the lab to take more test data. An example is having a Hybrid model of a SCCI backplane consisting of a PCB, Connector and SCCI ribbon cable. Later it is required that a longer SCCI cable is needed but you want to verify its effect on the system signal integrity. Since you already have the backplane hybrid model, you only need to create a measured based model of the SCCI cable, recompile it with the backplane model, to see its effect on the system signal integrity.



Example of OPEN TDR measurements to define physical section lossy models

Advantages for one port TDR measurements

The Open TDR measurement characterizes both DC and AC losses (skin effect and dielectric) as computed from the measured rise time degradation between incident and reflected waves. The extracted H-spice net model "captures" all interconnect AC/DC parameter values including the IC input self and mutual capacitance to a f-Farad accuracy. FA data such as PCB loss tangent can be also extracted from these measurements. Using new *multi-mode* hand probe technology and a true differential TDR allows for detecting mode change close to IC inputs (e.g. via) which can cause serious functional EMI failures. A recent introduction of a new 30 GHz multi-mode differential hand probe series called GigaProbes™ (www.gigaprobes.com), was used in the test case examples to demonstrate open TDR using virtual grounded differential probes to easily extract impedance and S-parameters.

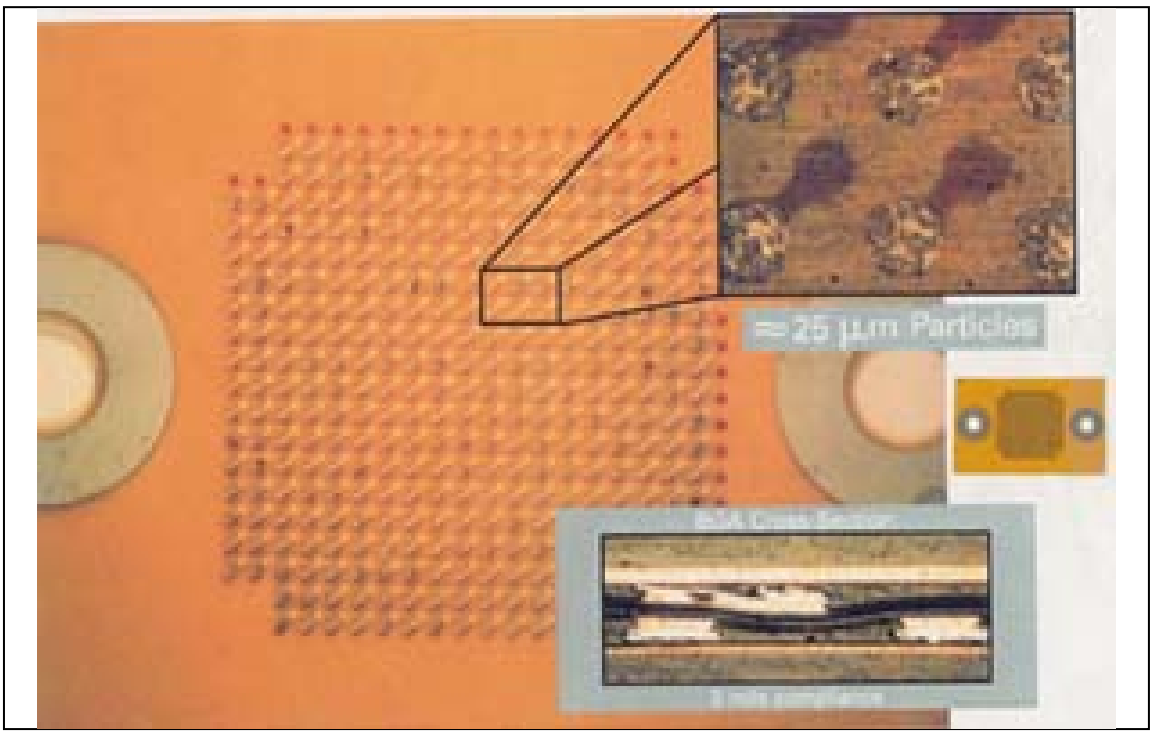
Gigaprobes™ New Product Description

DVT30-1MM GigaProbes™ is the worlds first Fully Balanced Differential multi-mode (100Ω Differential, 50Ω Single Ended) TDR hand probe for capturing 30GHz, ODD/EVEN impedance profiles. With a typical differential launch discontinuity of <20mv and a odd mode rise time of 20ps, these probes masks ~20mils of the device under test. This small discontinuity mask is most important when characterizing IC packages where net lengths can be very short. The DVT30-1MM comes with a set of ergonometric grips for comfortable hand probing and they easily attach to Probe Station micromanipulators; providing a 2 inch, low profile, wide band reach. The Signal-to-Signal pitch can be set to .5mm, 1mm or 2mm using a custom designed SMA wrench. The pitch can also be customized using other tools supplied in the DVT30-1MM GigaProbes™ accessory kit.

DVT30-1MM GigaProbes™ is the worlds first Fully Balanced Differential multi-mode (100Ω Differential, 50Ω Single Ended) TDR hand probe

Description of DUT: Diamond Partial Interconnect (DPI)

The Diamond Particle Interconnect surface mount BGA socket is a flex ridget board. This board is used as a chip carrier eeliminating LEAD solder balls with a nickel coated 100 GHz Diamond Interconnect which allows chips to be GLUE down to PCB's, increasing bandwidth. This military grade Diamond Interconnect is the latest application of nano-technology, preferred in life support systems. This controlled impedance material is electrically invisible, requires only 5 grams contact force, withstanding 1.5 million insertions and resists oil and dirt contaminates.



Diamond Particle Interconnect (DPI) socket shows PCB conformance

DUT Reference Setup for Z Measurements

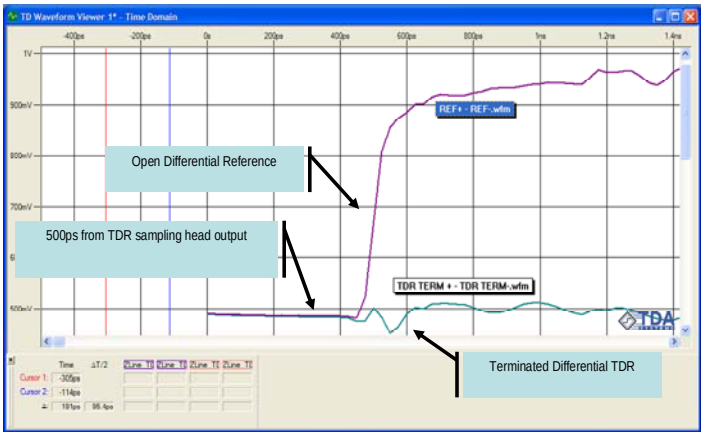
Key advantage to Tektronix TDR is that it launches two pulses (+/-) and it "measures" the "true" differential response. The VNA applies a frequency sweep in a round-robin format and "computes" a differential TDR response but never measures a true odd mode wave front propagation. GigaProbes™ is a twin line odd mode probe with built in precision 100 ohm reference to accurately calculate the impedance of the DUT.

What is a Reference Waveform?

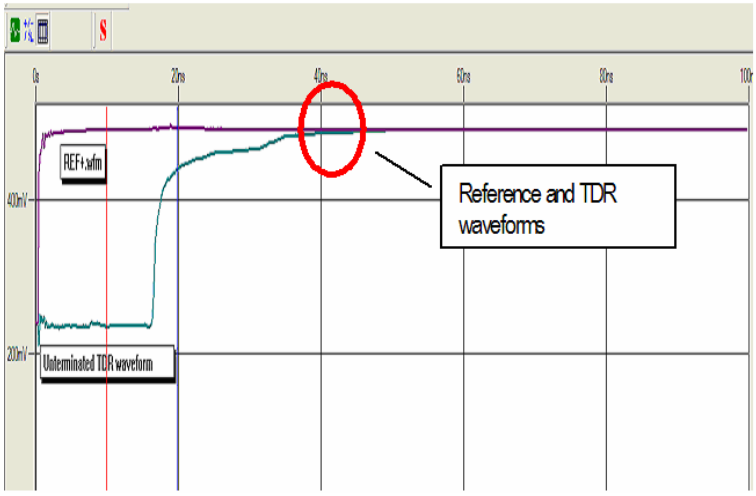
- It Is an Open TDR Measurement made prior to the DUT
- Needed for creating S-parameters, Impedance waveforms and Spice models

Creating an Reference Waveform

1. Move TDR Waveform to Left Side of TDR Screen
2. Place Reflection TDR pulse 1 division from left side of TDR display
3. Reference plane 500ps from the TDR Sampling head



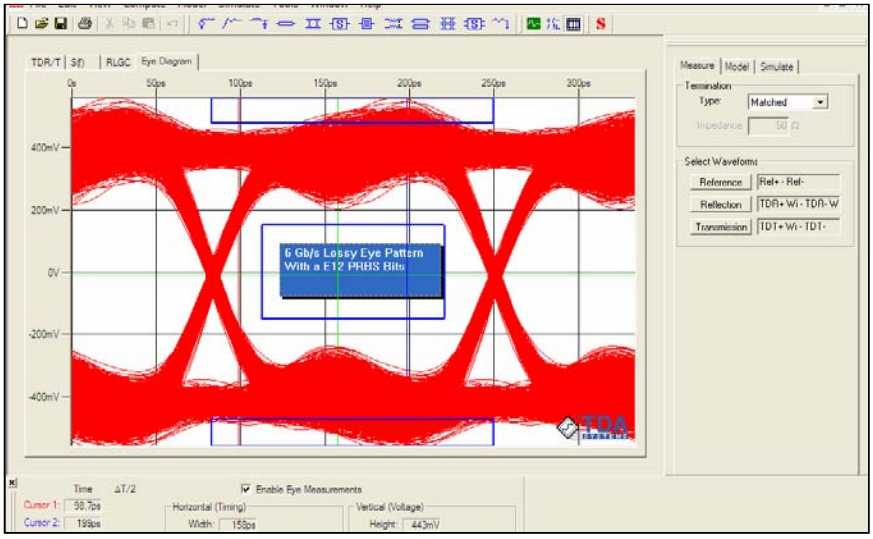
Example of a correct TDR Reference Launch



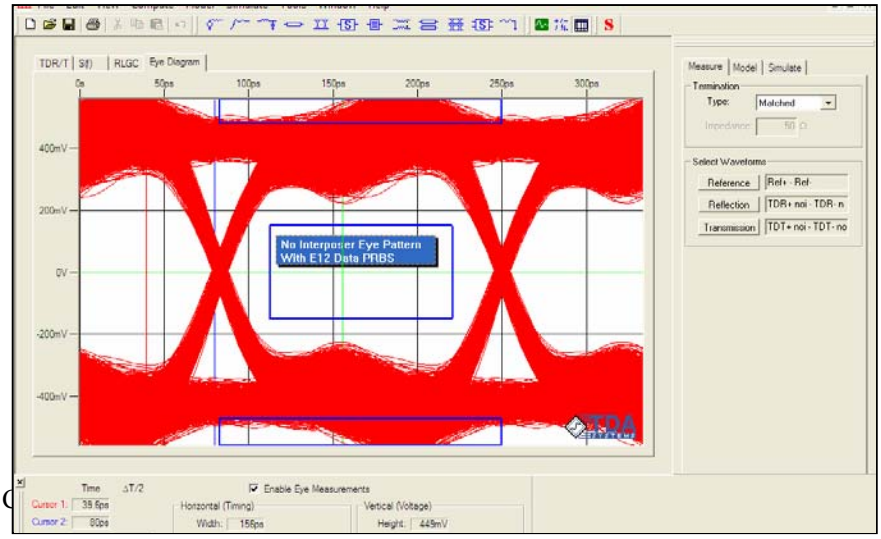
Correct TDR and Reference Settling Time

Measured DPI Eye Diagram Degradation

Shown below are eye patterns with and without DPI socket to measure the degradation effect for just the DPI Socket. There was only a 10mv or 5% eye degradation and a 1ps increase in jitter caused by DPI socket. Therefore the DPI socket is has no significant impact to the eye mask test margins.



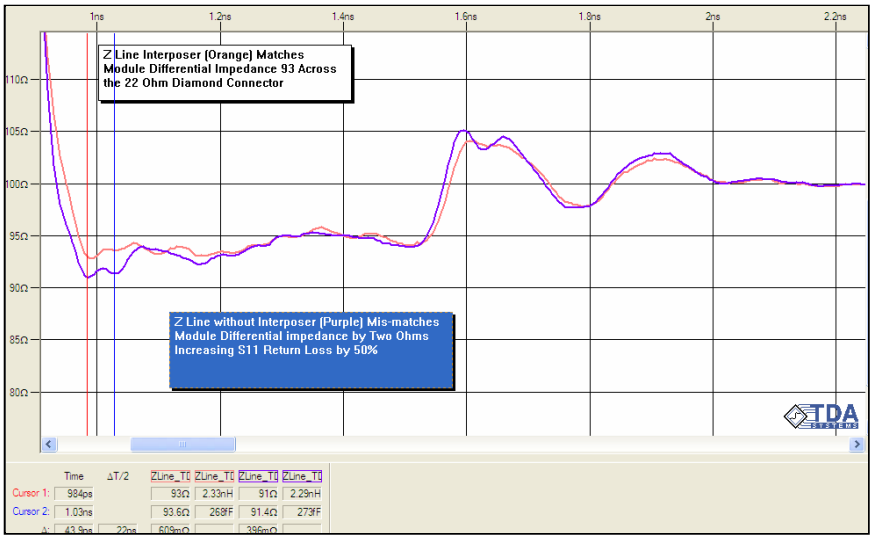
Eye Diagram for Connection with Diamond Interposer only <1% degradation



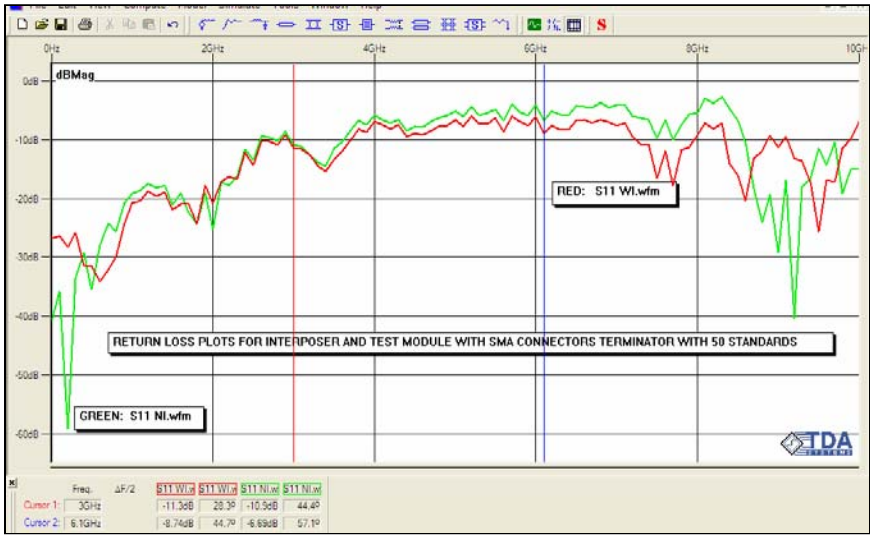
Eye Diamond without Diamond Connections is 449mv only 5mv larger

Diamond Interposer to Module Impedance Match

Shown below is the impedance comparison for differential signal pair on the test module. The interposer has a much better match to both the PCB and the transceiver IC onboard terminator. Most significant, the DPI shows no capacitive or inductive reactance. With uniform impedance profile, the DPI socket, decreased Return Loss by 3dB.



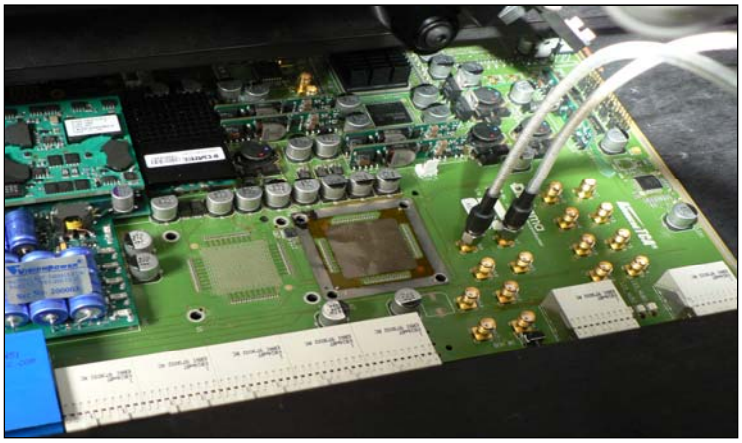
Impedance comparison shows 1 ohm series resistance with no significant Capacitive or Inductive Reactance



Return Loss for IC test board with Diamond Interpose shows 3dB enhancement with of high integrity contact even with Marginal PCB technology

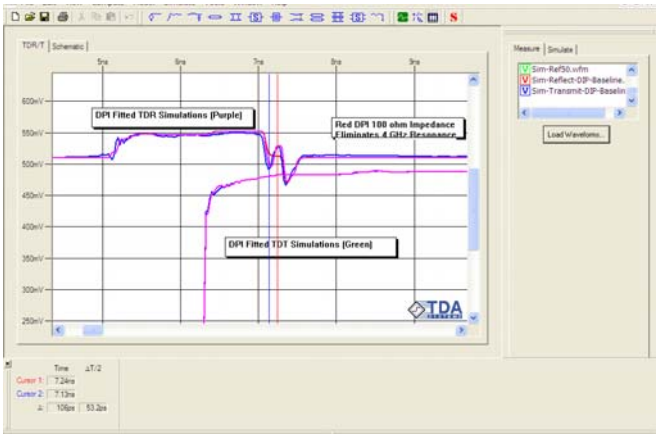
Two port transceiver s-parameters from One Port TDR

The photograph below shows a differential TDR connection to an IP transceiver port. We will characterize return loss using a one port TDR measurement. In this case the IC termination is matched. We need only to capture the reference and TDR waveforms to extract Return Loss, but a 2nd port is not available. Using time domain analysis, the input can be characterized in time domain and the insertion loss is extracted from TDT simulation. This is done after carefully fitting the Spice models to the Return loss and TDR measurements. The TDT and S21 were extracted from Hspice simulations.

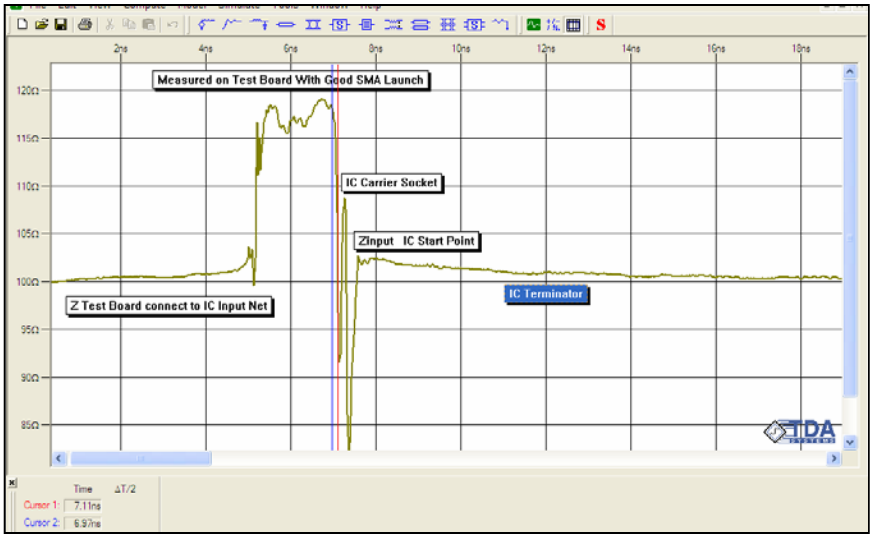


Photograph of IC test Board with a single port differential Connection
Internal to the IC is a Match termination for easy Return loss control

Shown below is the transceiver TDR measurement with optimized TRD/T simulations. Also shown in red is the 100 ohm, non reactive DPI socket. Note the input capacitance of this IC is so low that impedance only dips 20mv which makes for a very low return loss. Shown in the figure below is the insertion and return loss with and with out the DPI socket. This shows a 4 GHz resonance caused by the solder ball which fails the PCI return loss specification. The only want to get this to pass is to use the DPI socket which passes the return loss well beyond 12 GHz.



DPI No Reactance Socket Eliminates 4 GHz Resonance



Less than 10mv discontinuity at connections yields less than 5 ohm differential Impedance changes. Need better Chip carrier with no Connect reactance

Conclusions

The one port TDR to extract two port s-parameters was successfully demonstrated in these test cases and was so accurate that it resulted in discovery of a very subtle solder ball resonance that generically causes return loss failure below 6 GHz for BGA packages. This was eliminated by introducing a high bandwidth non reactive Diamond Particle Interconnect socket with only 1 ohm series DC resistance.

Using the same calibrations standards for TDR and VNA it has been shown that TDR measured is as accurate VNA two port S parameter measurements. This is critically important for IP application since only one test port is available. As a result, the eye patterns generated by this technique are very accurate because of the wide band measurement from DC to measurement Instrument f-max. For this approaches 30 Gb/s or eye diagrams or bit times well less than 40ps. Therefore, a 2x faster (e.g. <20ps) TDR pulse would be required to characterize copper interconnect eye patterns with bit time of less than 25ps or data rates grater than 40Gb/s

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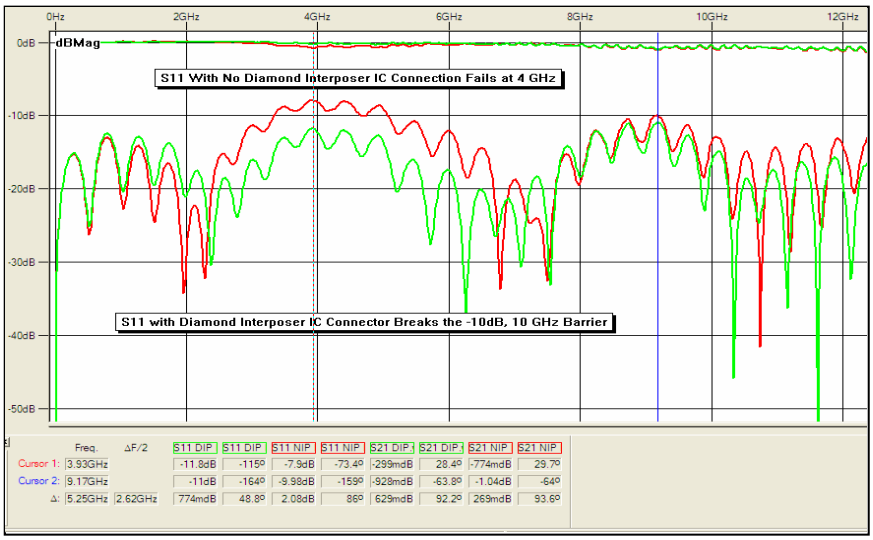

Insertion and return loss showing 4 GHz resonance at BALL with out DPI Socket causing PCIX Return Loss failure below 6 GHZ without DPI Socket