

In-Situ De-embedding (ISD)

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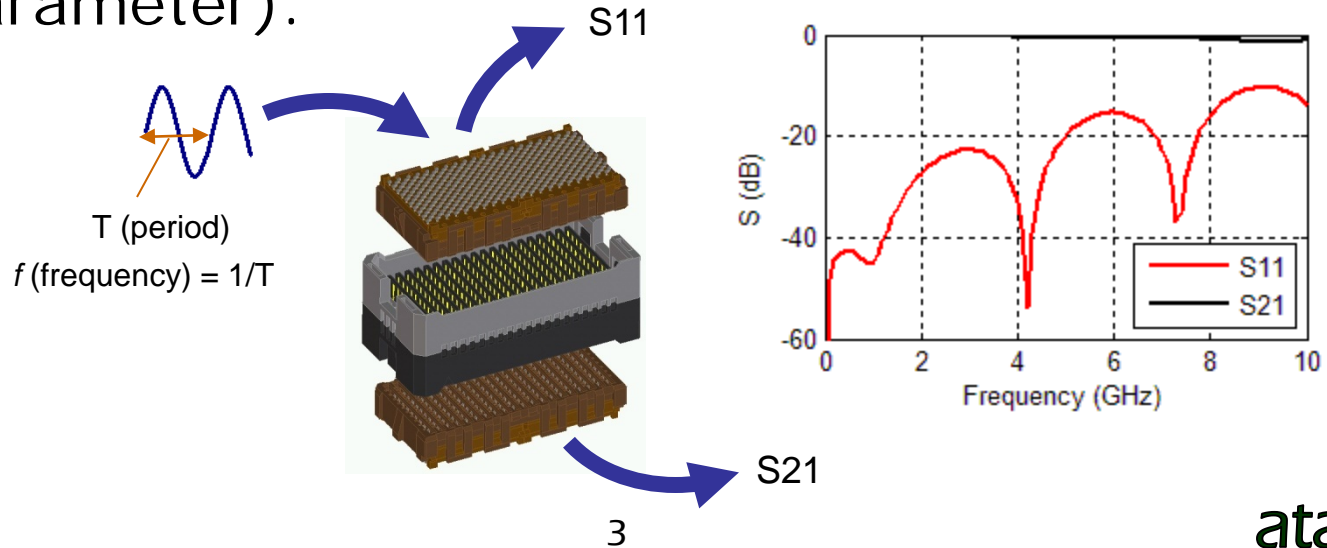
January 31, 2018

Outline

- What is causality
- What is In-Situ De-embedding (ISD)
- Comparison of ISD results with simulation and other tools
- How non-causal de-embedding affects connector compliance testing
- How to extract accurate PCB trace attenuation that is free of spikes and glitches
- How to extract a PCB's material property (DK, DF, roughness) by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded PCB traces

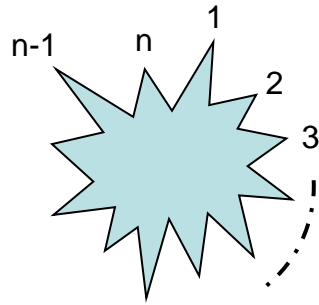
VNA and S parameter

- Vector network analyzer (VNA) is an equipment that launches a sinusoidal waveform into a structure, varies the period (or frequency) of waveform, and lets us observe the transmitted and reflected wave as “frequency-domain response”.
- Such frequency-domain response, when normalized to the incident wave, is called scattering parameter (or, S parameter).



What is S parameter

- For an n-port (or I/O) device, S parameter is an n x n matrix:



$$[S_{ij}]_{n \times n} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ S_{n1} & S_{n2} & S_{n3} & \dots & S_{nn} \end{bmatrix}$$

- S_{ij} is called the S parameter from Port j to Port i .
- S_{ij} has a unique property that its magnitude is less than or equal to 1 (or, 0 dB) for a passive device.

$$|S_{ij}| \leq 1$$

$$S_{ij} (dB) = 20 \times \log_{10} |S_{ij}| \leq 0 \text{ dB}$$

What is a Touchstone (.sNp) file

- S parameter at each frequency is expressed in Touchstone file format.

```
! Total number of ports = 4
! Total number of frequency points = 800
# GHZ S DB R 50
0.025 -36.59296 48.77486 -41.40676 79.91354 -0.08648679 -6.544144 -49.50045 -105.618
-41.39364 79.94686 -36.35592 51.52433 -49.4886 -105.5124 -0.09038406 -6.527076
-0.08421237 -6.537903 -49.44814 -105.644 -36.0317 49.60022 -41.37105 79.91856
-49.44393 -105.8186 -0.09834136 -6.542909 -41.36758 79.9318 -36.05645 48.98348
0.05 -32.22576 48.03161 -35.59394 74.15976 -0.1277169 -12.82876 -43.90183 -112.0995
-35.58736 74.16304 -32.12694 50.92389 -43.90926 -112.0764 -0.132402 -12.7985
-0.1242117 -12.82302 -43.89 -112.0248 -32.10987 50.3115 -35.56998 74.078
-43.88424 -112.0517 -0.1381616 -12.80199 -35.56758 74.06782 -31.94136 50.49276
0.075 -29.88861 42.02766 -32.19713 68.06704 -0.1589249 -19.05252 -40.67476 -118.8188
-32.19116 68.0941 -29.7086 45.41557 -40.63857 -118.837 -0.1635606 -19.01593
-0.1603356 -19.0376 -40.63557 -118.8543 -29.89064 47.63852 -32.16917 67.94677
-40.65711 -118.8021 -0.1737256 -19.02956 -32.16865 67.93389 -29.65444 46.15548
: : :
```

in GHz

S param

in dB and phase angle

Reference impedance

0.075

Frequency in GHz

S11, S12, ..., S44 in dB and phase angle

What is causality

cau·sal·i·ty

/kô'zalədē/

noun

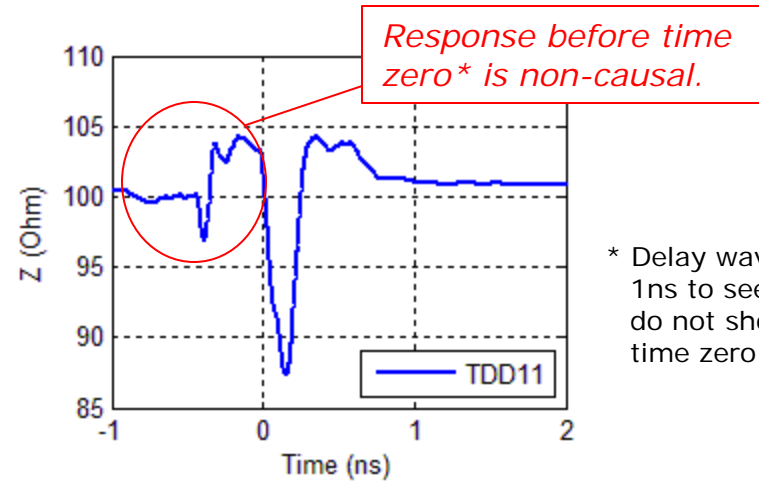
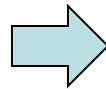
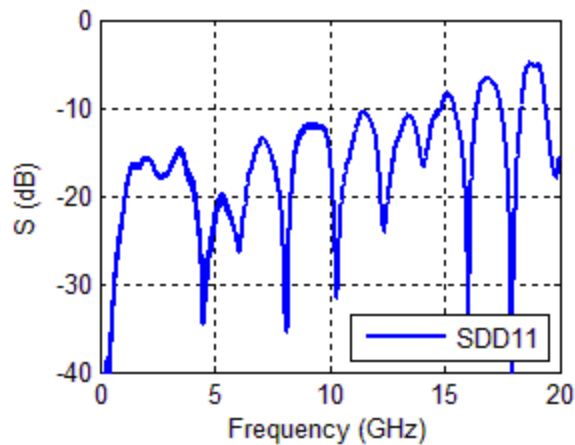
1. the relationship between cause and effect.
2. the principle that everything has a cause.

In other words:

Can not get something from nothing.

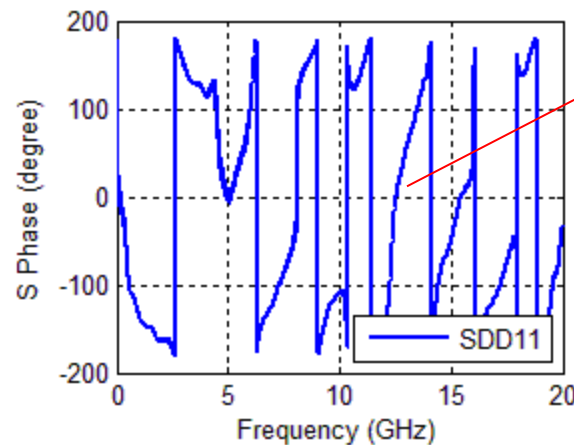
How to identify non-causal S parameter

- Convert S parameter into TDR/TDT.



* Delay waveform by 1ns to see if tools do not show before time zero.

- Check phase angle.



Counterclockwise phase angle is non-causal.

Why does S parameter violate causality

- Measurement error (**de-embedding**), simulation error (**material property**) and **finite bandwidth** of S parameter all contribute to non-causality.
- Kramers-Kronig relations require that the real and imaginary parts of an analytic function be related to each other through Hilbert transform:

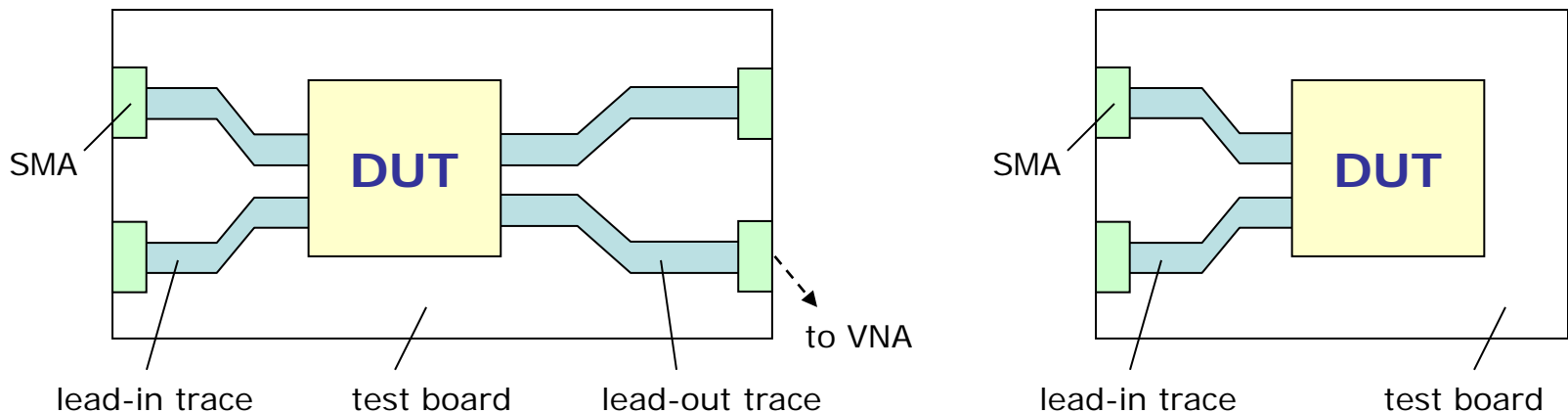
$$\Psi(\omega) = \Psi_R(\omega) + j\Psi_I(\omega)$$

$$\Psi_R(\omega) = \frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_I(\omega')}{\omega' - \omega} d\omega'$$

$$\Psi_I(\omega) = -\frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_R(\omega')}{\omega' - \omega} d\omega'$$

What is de-embedding

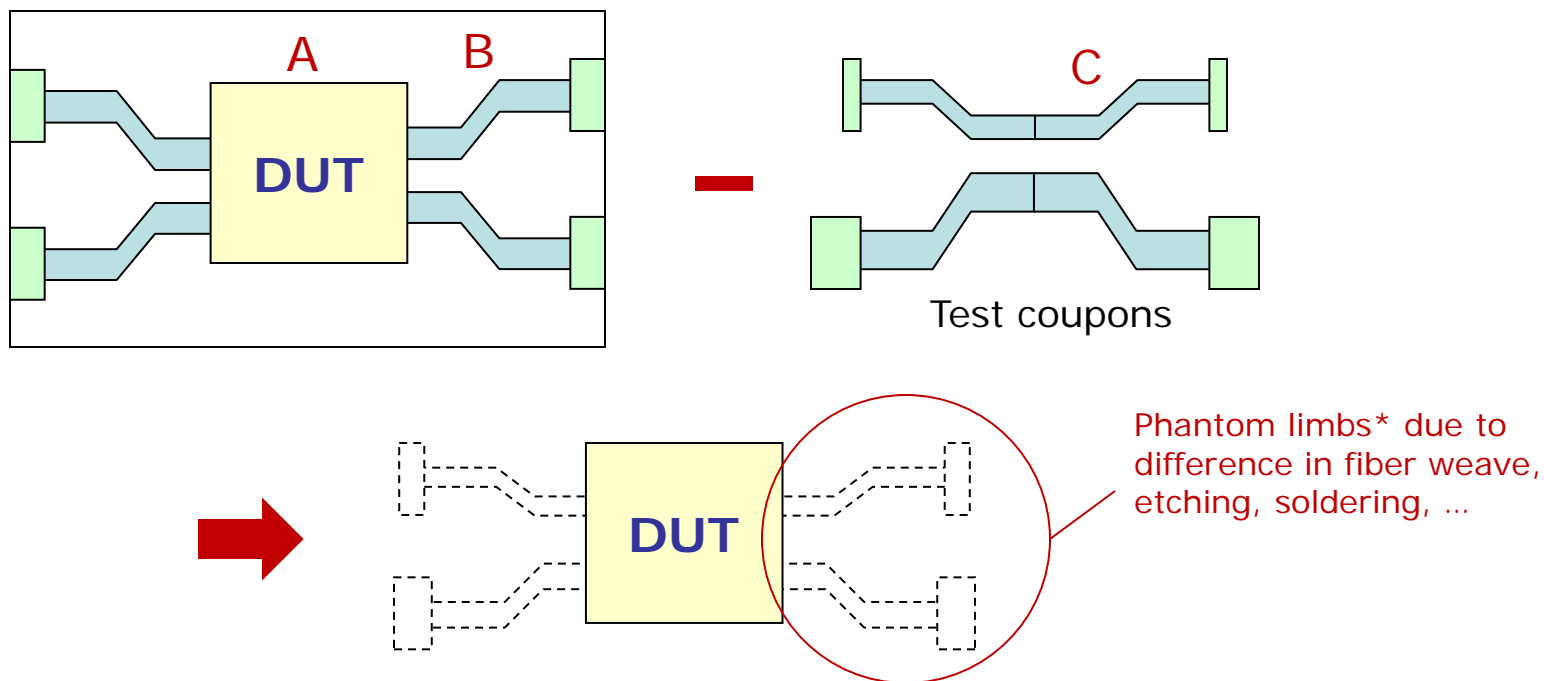
- To remove the effect of fixture (SMA connector + lead-in/out) and extract the S parameter of DUT (device under test).



- The lead-ins and lead-outs don't need to look the same.
- There may even be no lead-outs (e.g., package).

Why do most de-embedding tools give causality error

- Most tools use test coupons directly for de-embedding, so difference between actual fixture and test coupons gets piled up into DUT results.



* <http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations> by Eric Bogatin

What is In-Situ De-embedding (ISD)

- Use “2x thru” or “1x open / 1x short” as reference and de-embed fixture's actual impedence through numerical optimization.

In Situ

ISD by AtaiTec (www.ataitec.com) Version 2017.08

SI tools Plot S param Plot TDR Configuration Run Help

In Situ De-Embedding

Test Coupon

2x Thru 1x Open + 1x Short
 1x Open 1x Short

Select Touchstone File (2x Thru) 1

D:\Demo\Examples\ISD_Line2x.s2p

Split 2x Thru directly for de-embedding

Fixture + DUT 2

Select Touchstone File

D:\Demo\Examples\ISD_SMA_to_SMA.s4p

Port sequence

1 to N on left; N+1 to 2N on right
 1, 3, 5, ... on left; 2, 4, 6, ... on right
 All ports are on the left side

Optional

Scaling for lead-in flight time
Scaling for lead-in attenuation
Flight time for DUT + lead-ins ps
Max. frequency to de-embed GHz

Enforce passivity for test coupon (& fixture)
 Convert to differential signal
 Active DUT Plot figures for DUT

Mode: Accurate Fast
Ports to skip: None Left Right
 Specified:

Coupling among de-embedding traces
 None Weak Strong

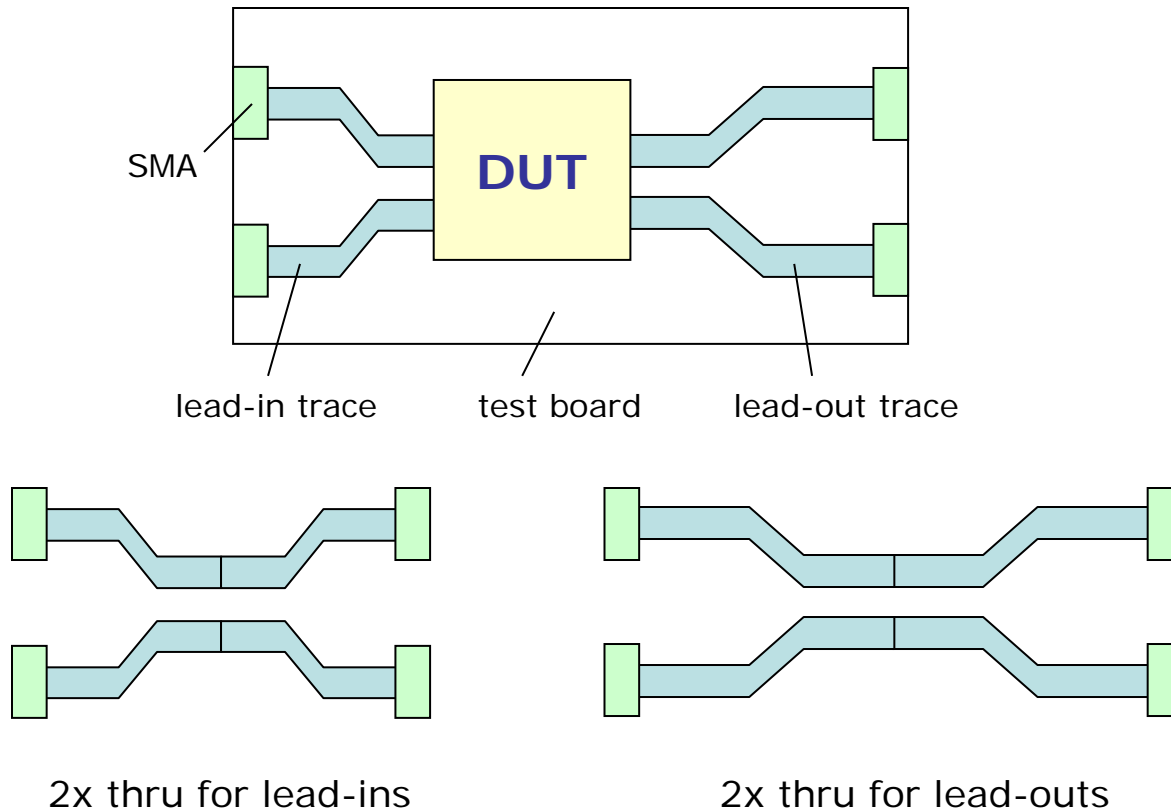
Files created:

D:\Demo\Examples\ISD_SMA_to_SMA.s4p_left_DUT.s4p
D:\Demo\Examples\ISD_SMA_to_SMA.s4p_right_DUT.s4p
D:\Demo\Examples\ISD_SMA_to_SMA.s4p_DUT.s4p

3

What is "2x thru"

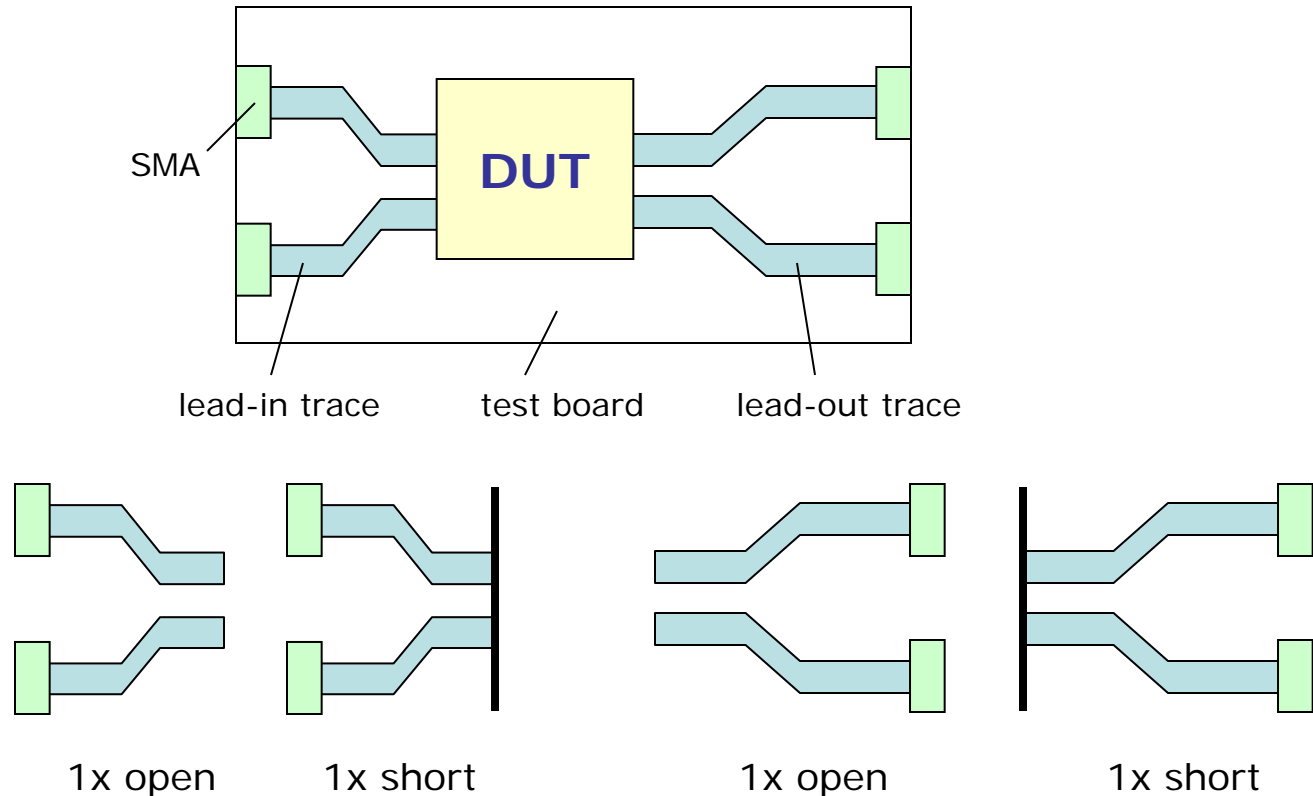
- "2x thru" is 2x lead-ins or lead-outs.



2 sets of "2x thru" are required for asymmetric fixture.

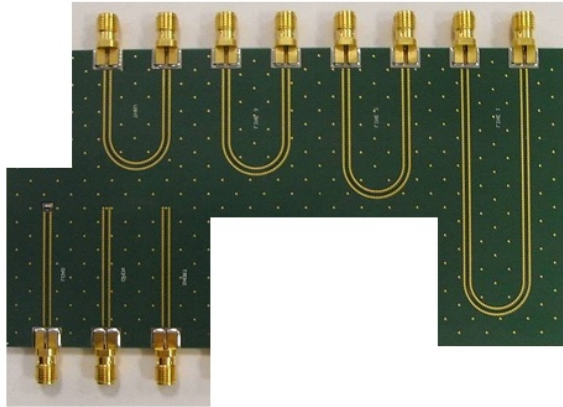
What is "1x open / 1x short"

- "1x open / 1x short" is useful when "2x thru" is not possible (e.g., connector vias, package, ...).



Why ISD is more accurate and saves \$\$\$

TRL calibration board



- More board space - Multiple test coupons are required.
- Test coupons are used directly for de-embedding.
- All difference between calibration and actual DUT boards gets piled up into DUT results.
- Expensive SMAs, board materials (Roger) and tight-etching-tolerance are required.
 - Impossible to guarantee all SMAs and traces are identical (consider weaves, etching, ...)
- Time-consuming manual calibration is required.
 - Reference plane is in front of DUT.

ISD test coupon



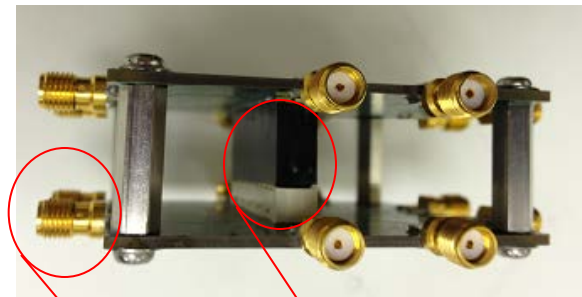
- Only one 2x thru test coupon is needed.
- Test coupon is used only for reference, not for direct de-embedding.
- Actual DUT board impedance is de-embedded.
- Inexpensive SMAs, board materials (FR4) and loose-etching-tolerance can be used.
- ECal can be used for fast SOLT calibration.
 - Reference plane is in front of SMA.
 - De-embedding requires only two input files: 2x thru and DUT board (SMA-to-SMA) Touchstone files.
 - More information: Both de-embedding and DUT files are provided as outputs.

* TRL = Thru-Reflect-Line

Example 1: Mezzanine connector

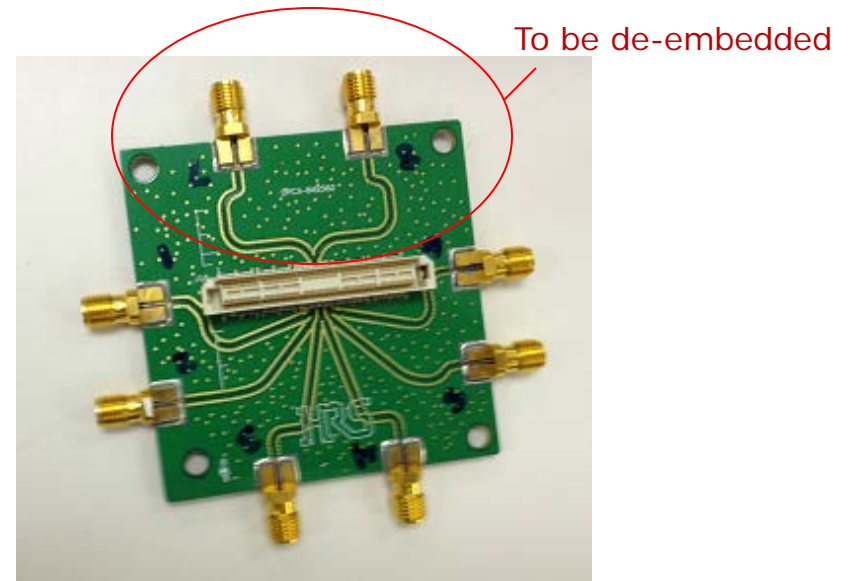
ISD vs. TRL

- In this example, we will use ISD and TRL to extract a mezzanine connector and compare their results.



SMA

Mezzanine
connector
(DUT)



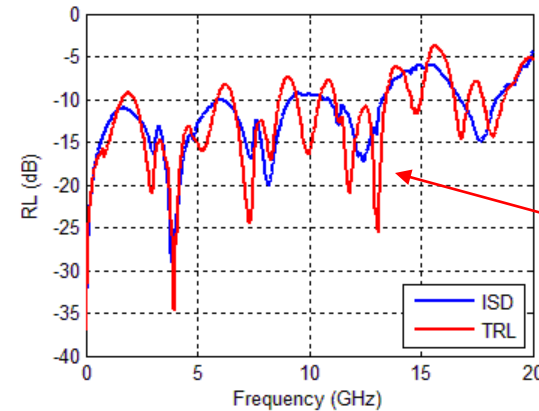
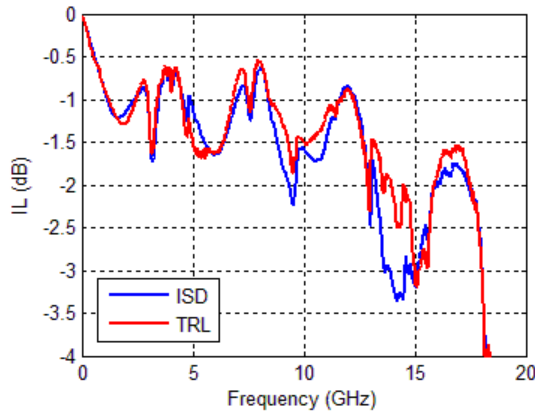
To be de-embedded

*Courtesy of Hirose Electric

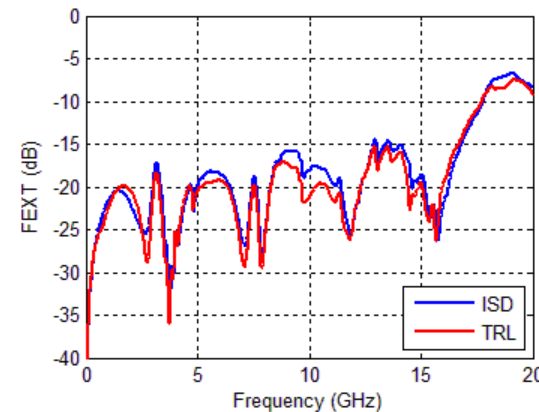
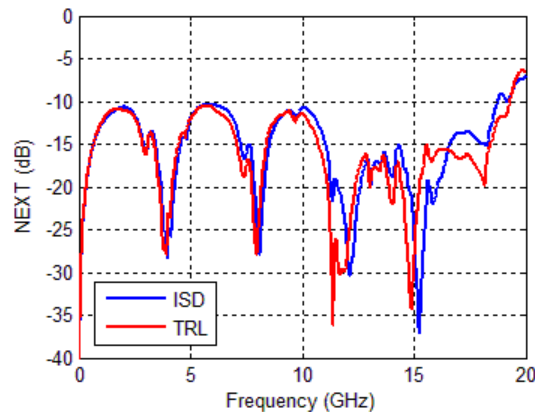
DUT results after ISD and TRL

Which one is more accurate?

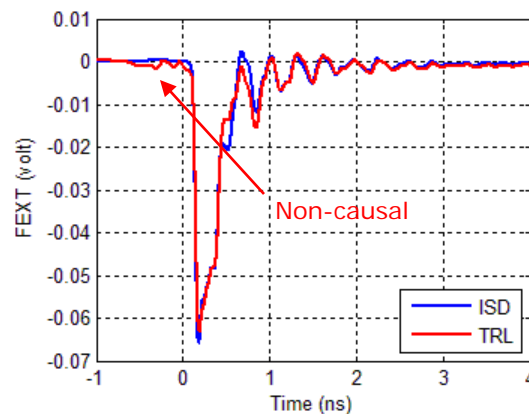
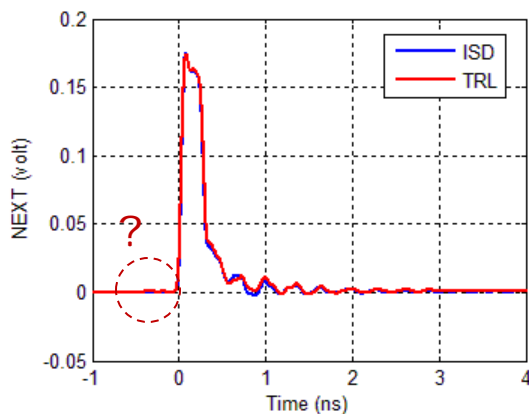
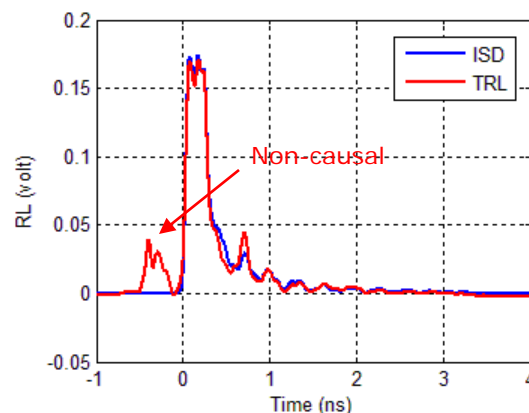
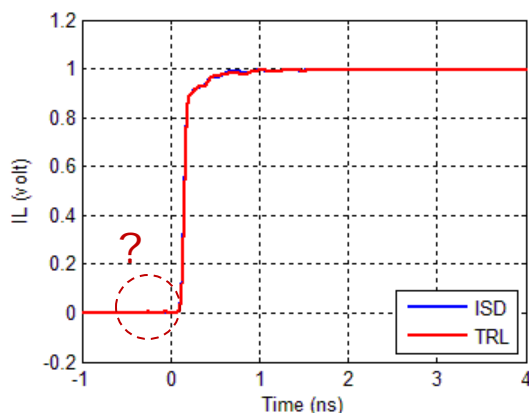
- TRL gives too many ripples in return loss (RL) for such a small DUT.



Non-causal ripples



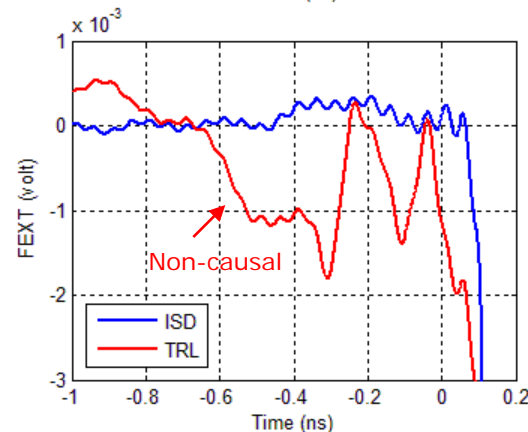
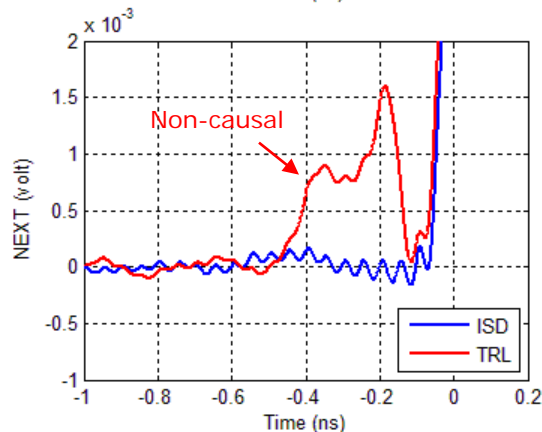
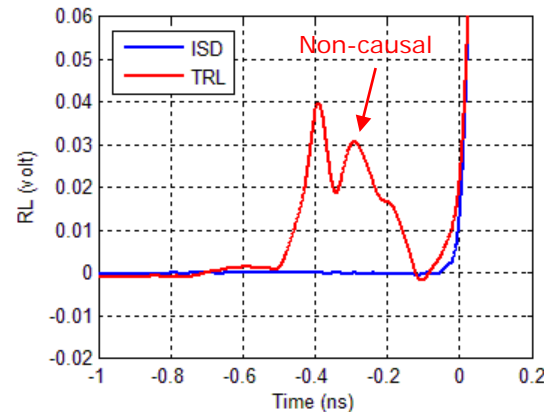
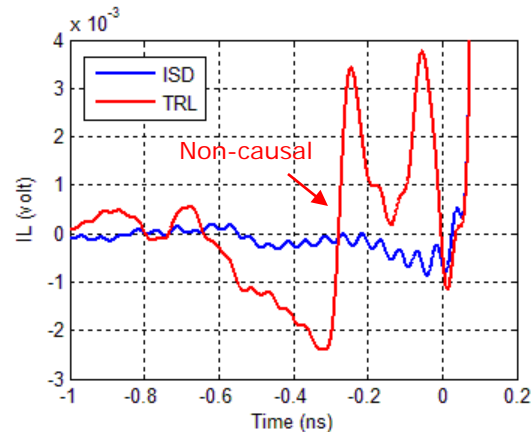
Converting S parameter into TDR/TDT shows non-causality in TRL results



Rise time = 40ps (20/80)

Zoom-in shows non-causal TRL results in all IL, RL, NEXT and FEXT

- TRL causes time-domain errors of 0.38% (IL), 25.81% (RL), 1.05% (NEXT) and 2.86% (FEXT) in this case*.

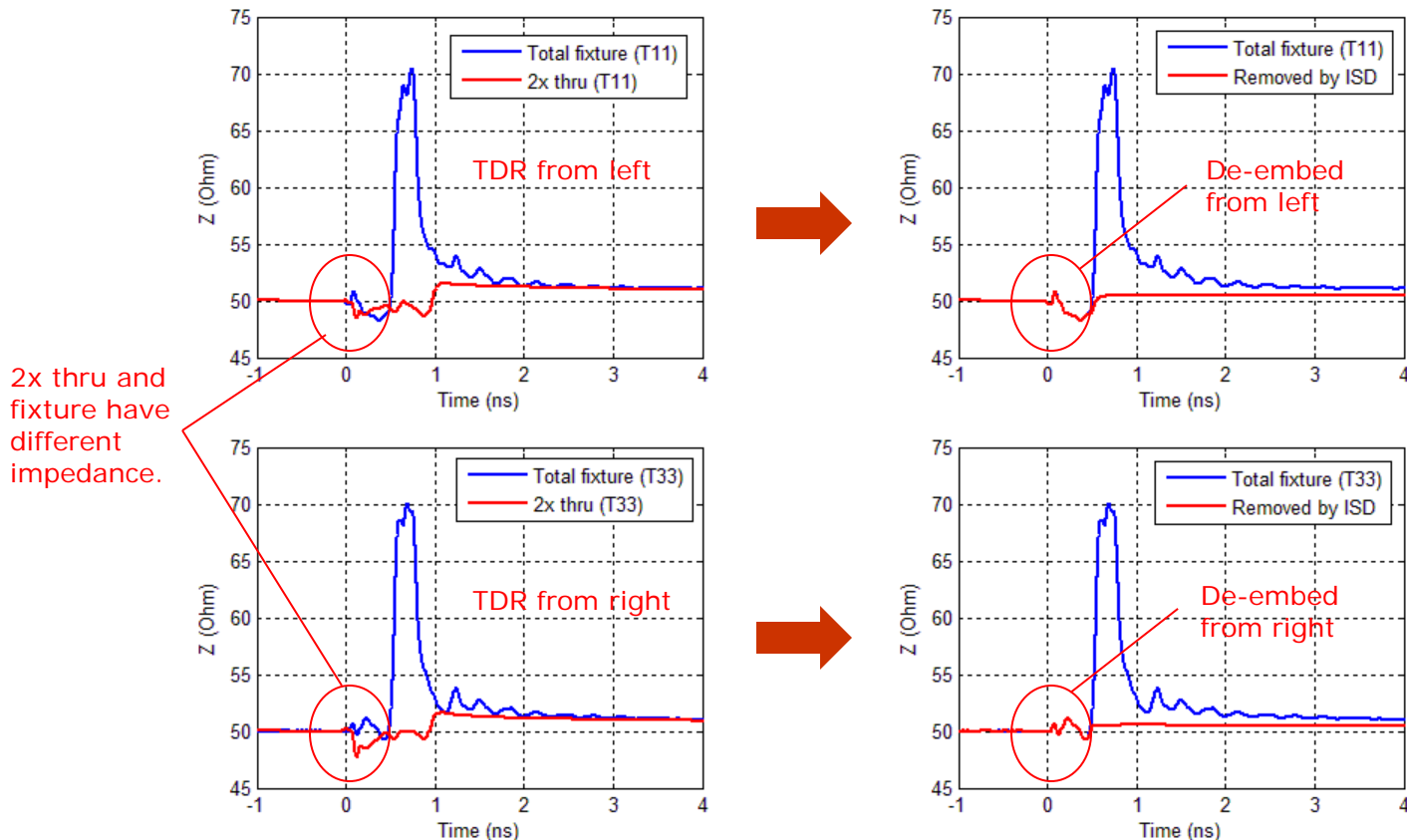


* The percentage is larger with single-bit response and/or faster rise time.

Rise time = 40ps (20/80)

How did ISD do it?

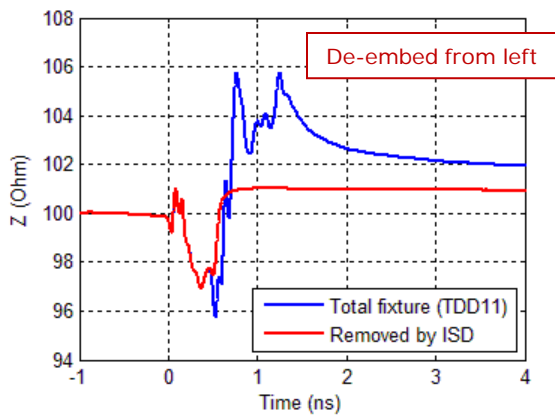
- Through numerical optimization, ISD de-embeds fixture's impedance exactly, independent of 2x thru's impedance.



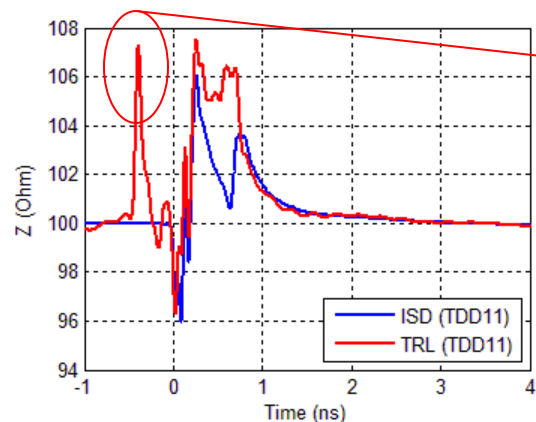
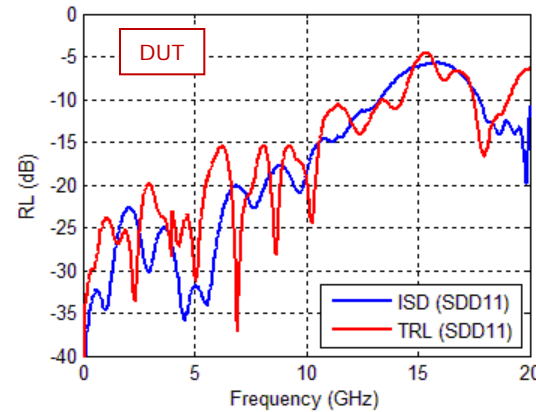
Rise time = 40ps (20/80)

TRL can give huge error in SDD11 even with small impedance variation*

- ISD is able to de-embed fixture's differential impedance with only a single-trace 2x thru.



* The impedance variation between 2x thru and fixture is less than 5%. (See previous slide.)

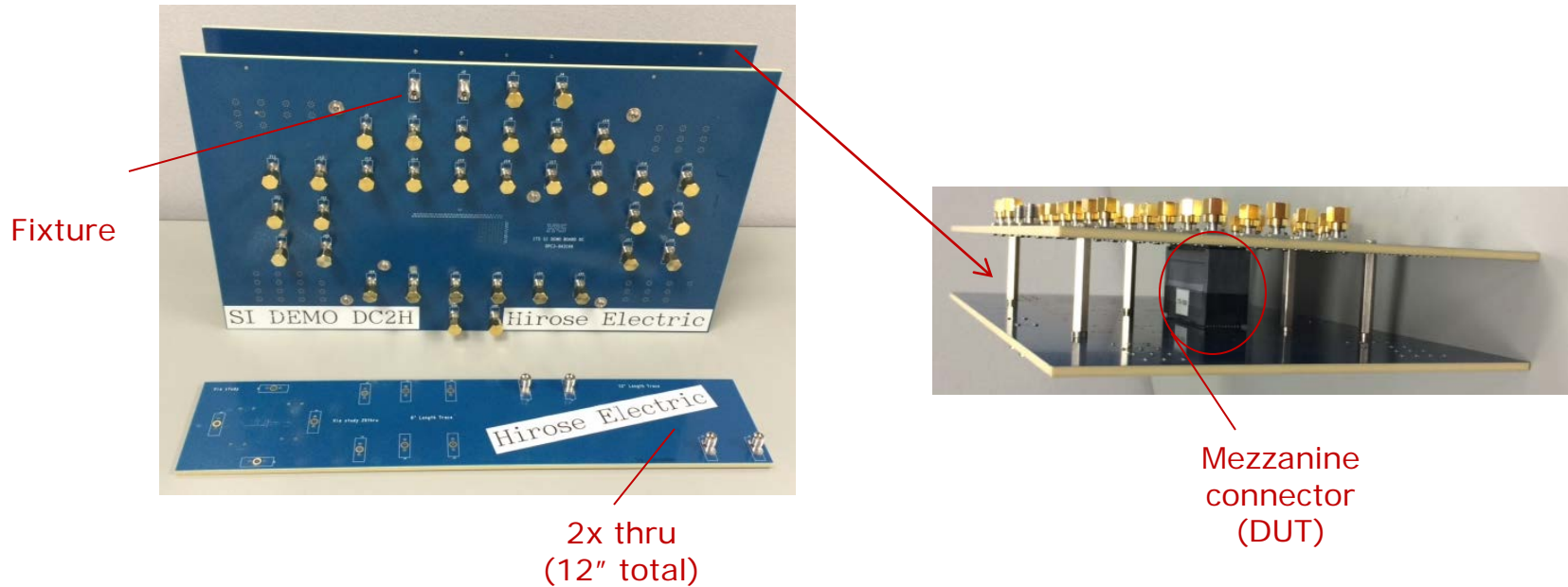


Rise time = 40ps (20/80)

Example 2: Mezzanine connector

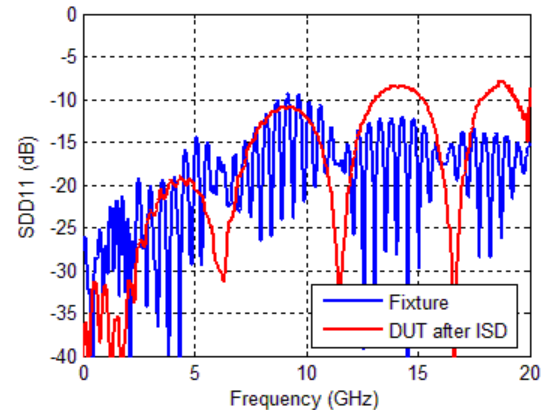
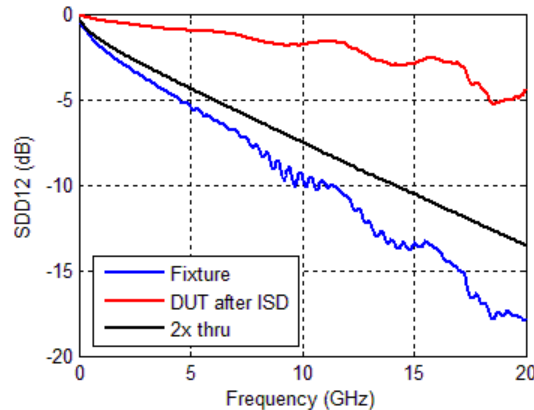
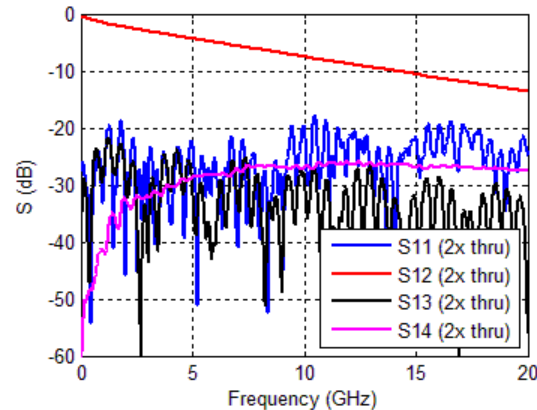
Extracting DUT from a large board

- TRL is impractical for de-embedding large and coupled lead-ins/outs.



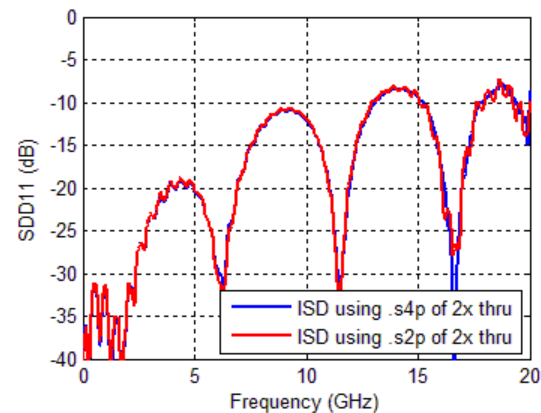
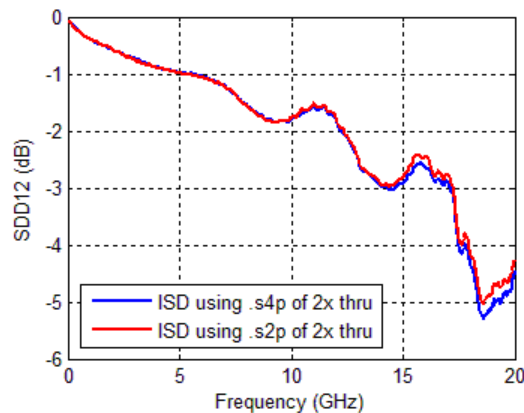
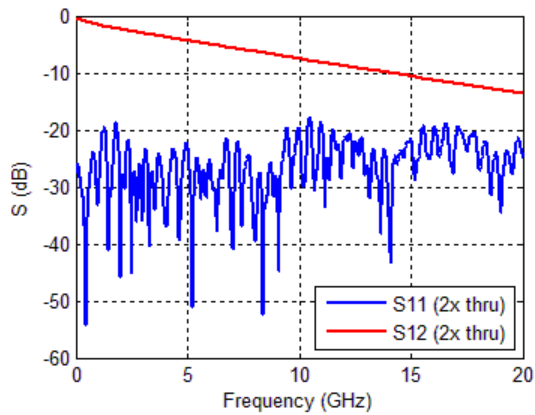
ISD can use a .s4p file of 2x thru for de-embedding

- TRL would have required many long and coupled traces.



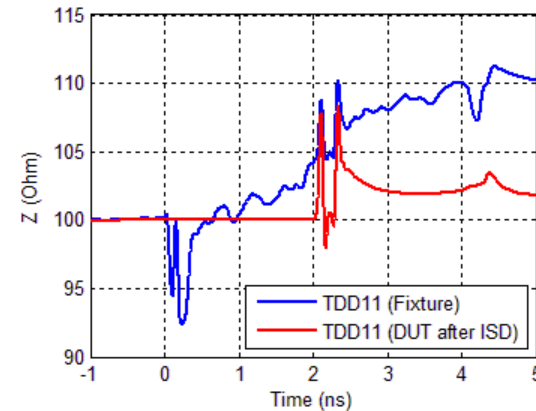
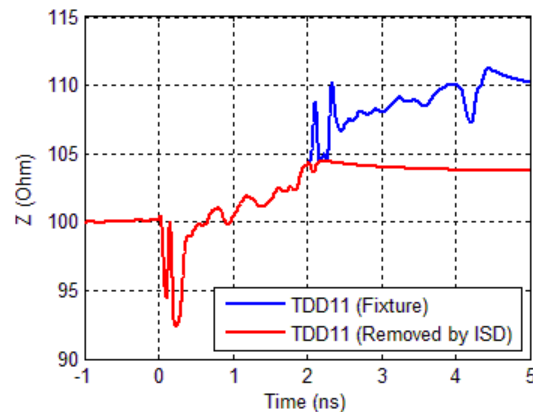
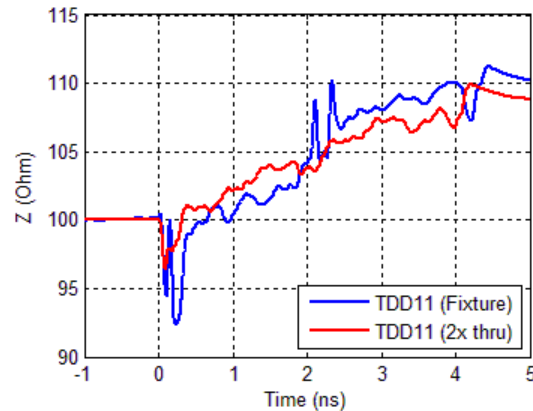
ISD can even use a .s2p file of 2x thru to de-embed crosstalk...

- And the results are similar!



ISD allows a large demo board to double as a characterization board

- ISD de-embeds fixture's impedance regardless of 2x thru's impedance.

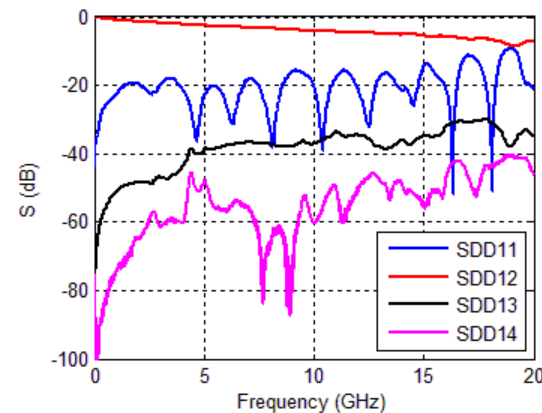
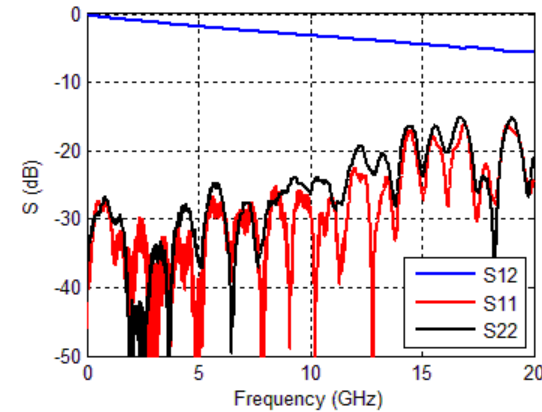
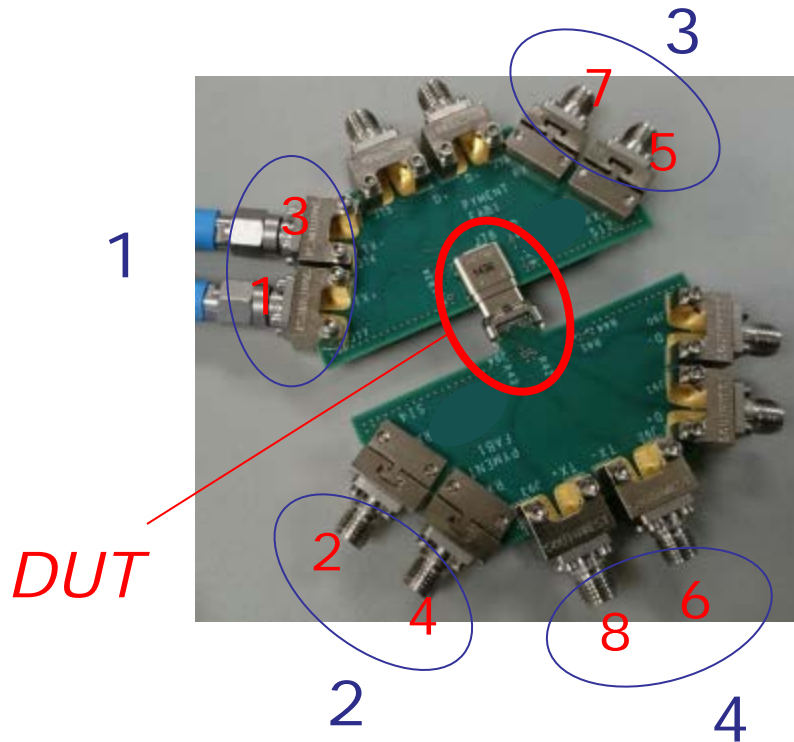


Rise time = 40ps (20/80)

Example 3: USB type C mated connector

ISD vs. Tool A

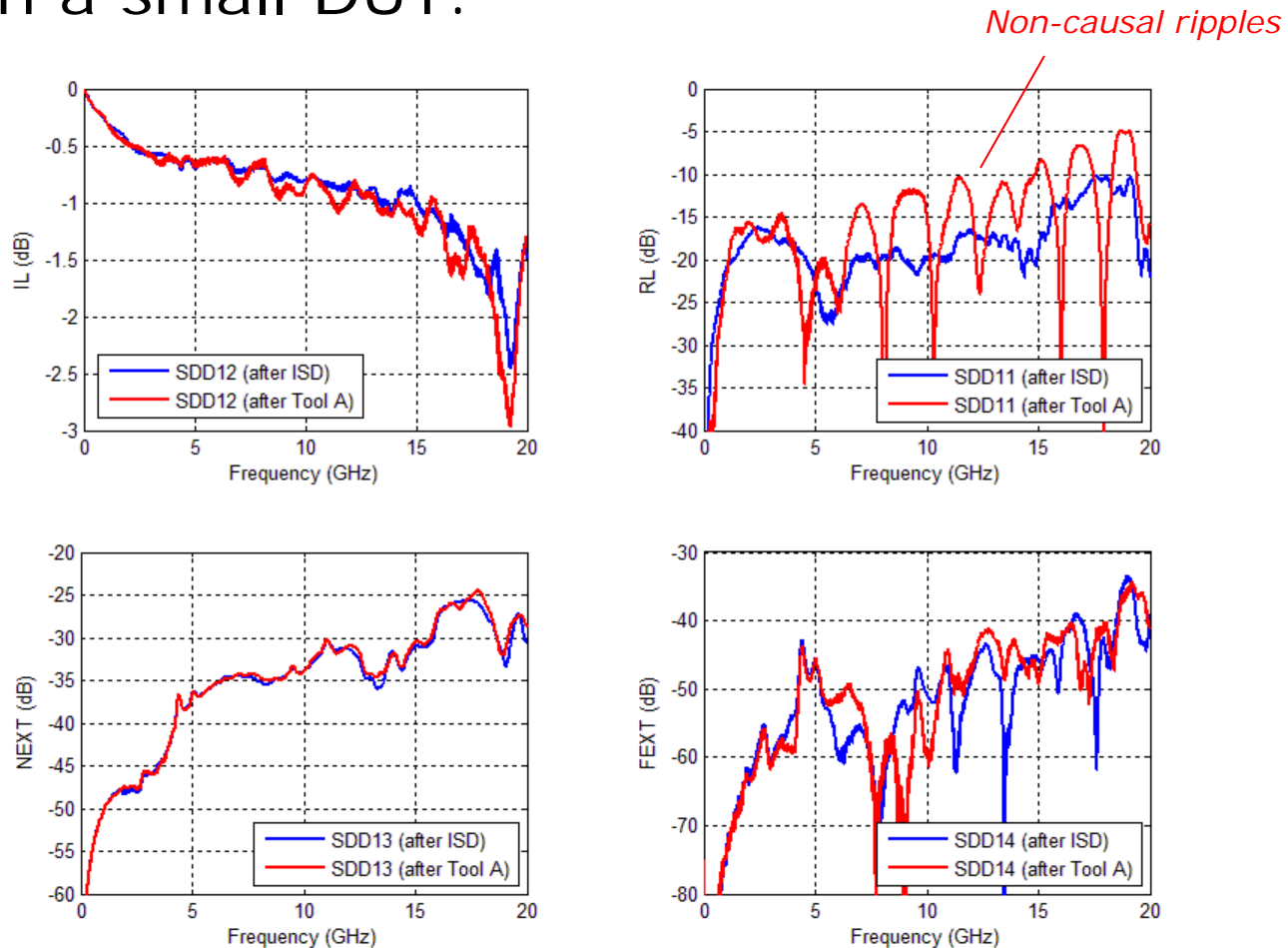
- Good de-embedding is crucial for meeting compliance spec.



DUT results after ISD and Tool A

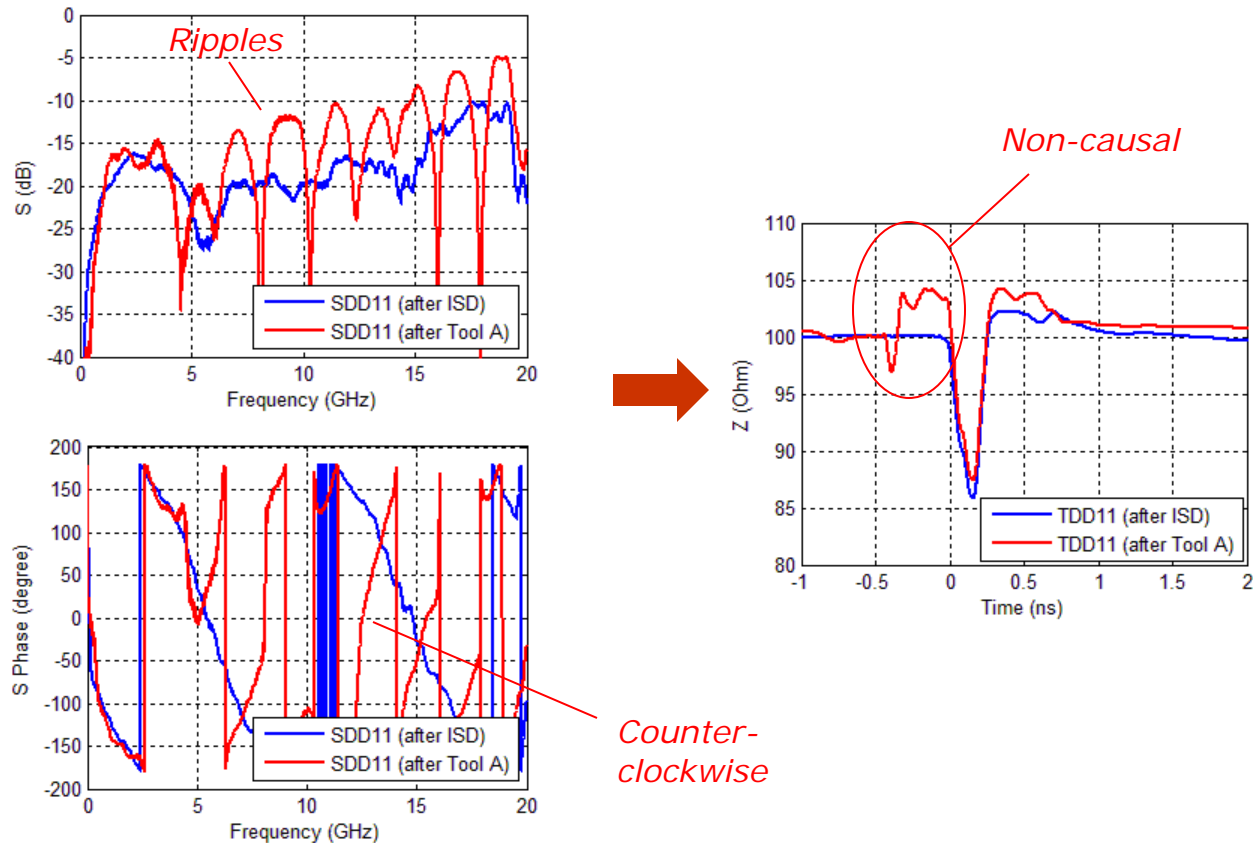
Which one is more accurate?

- Tool A gives too many ripples in return loss (RL) for such a small DUT.



Converting S parameter into TDR/TDT shows non-causality in Tool A results

- Counter-clockwise phase angle is another indication of non-causality.

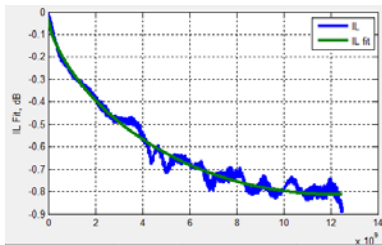


De-embedding affects pass or fail of compliance spec.

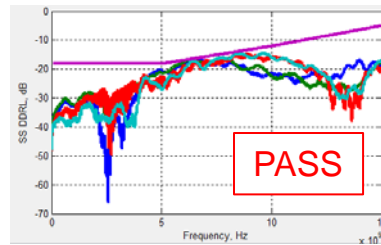
- ISD improves IMR and IRL (from compliance tool).

ISD

	Value (Pass/Fail)
ILfit@2.5GHz	-0.4
ILfit@5.0 GHz	-0.6
ILfit@10.0GHz	-0.8
IMR	-45.1
IRL	-23.2
INEXT	-41.5
IFEXT	-49.2
SCD12/SCD21	-23



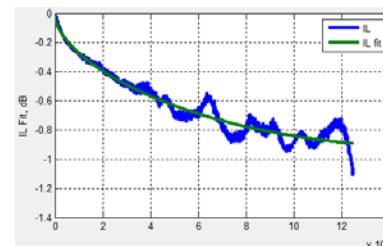
IL



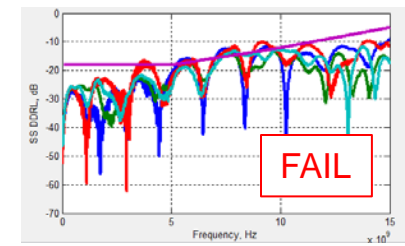
RL

Tool A

	Value (Pass/Fail)	Spec
ILfit@2.5GHz	-0.4	-0.6
ILfit@5.0 GHz	-0.6	-0.8
ILfit@10.0GHz	-0.9	-1.0
IMR	-43.7	-40
IRL	-20.8	-18
INEXT	-41.5	-44
IFEXT	-49.3	-44
SCD12/SCD21	-23.2	



IL

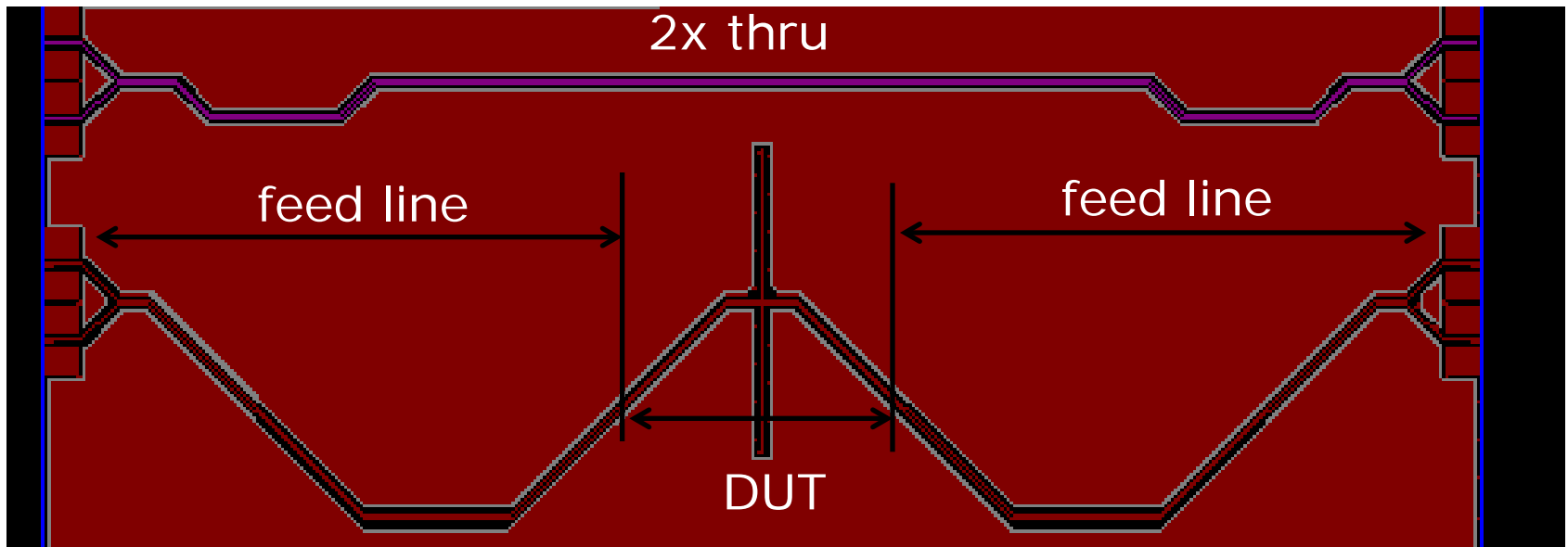


RL

Example 4: Resonator

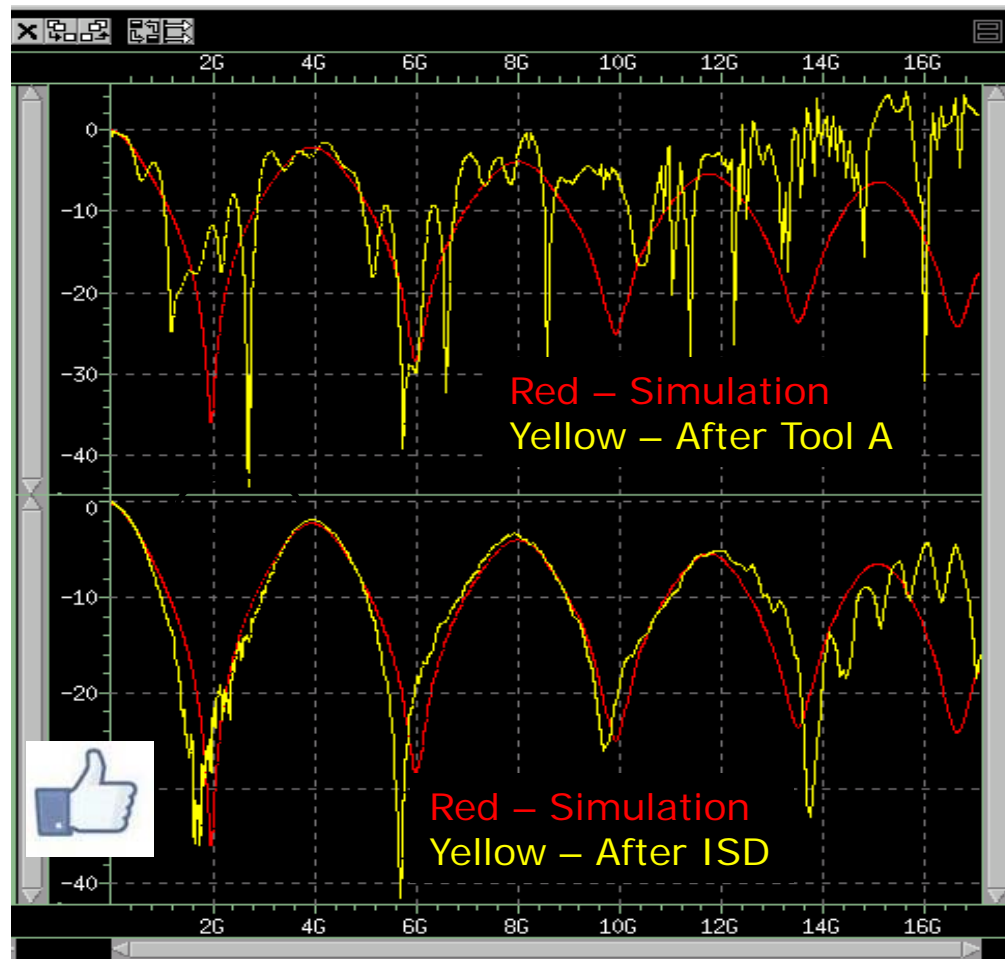
ISD vs. Tool A vs. simulation

- Good de-embedding is crucial for design verification (i.e., correlation) and improvement.



SDD11

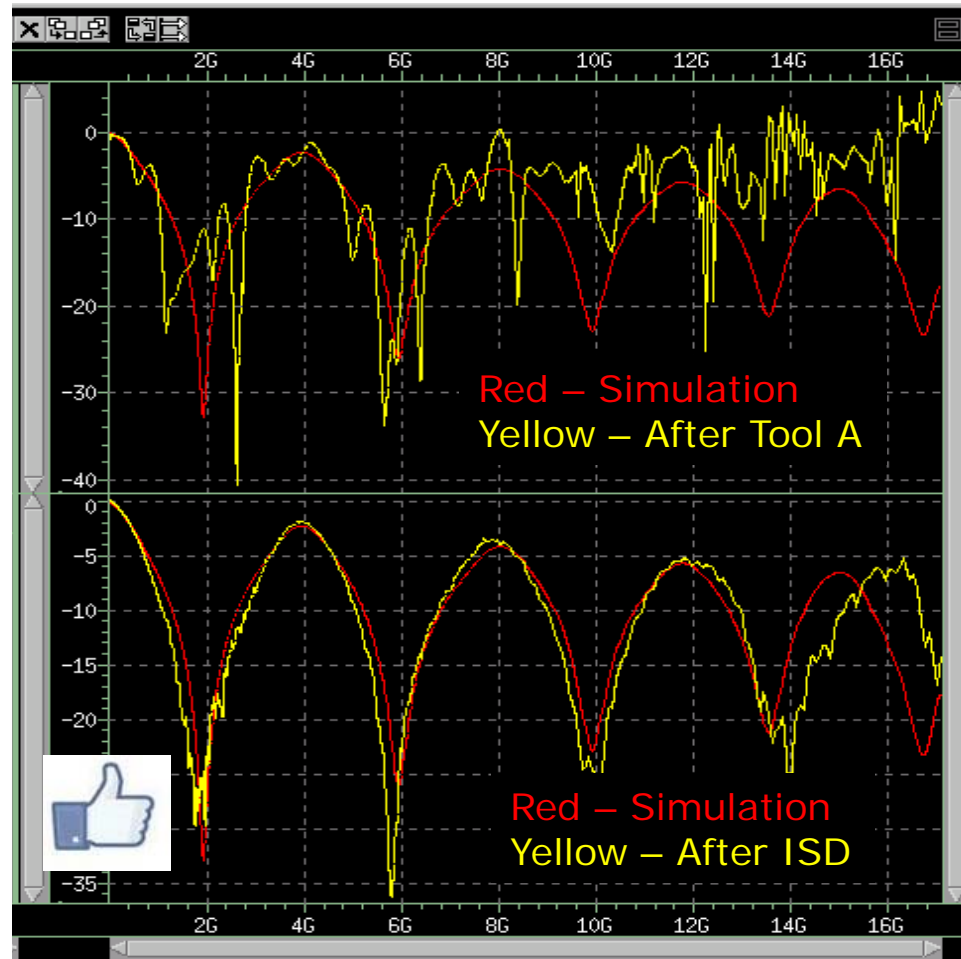
ISD correlates with simulation



SCC11

ISD correlates with simulation

- Good correlation is crucial for design improvement.



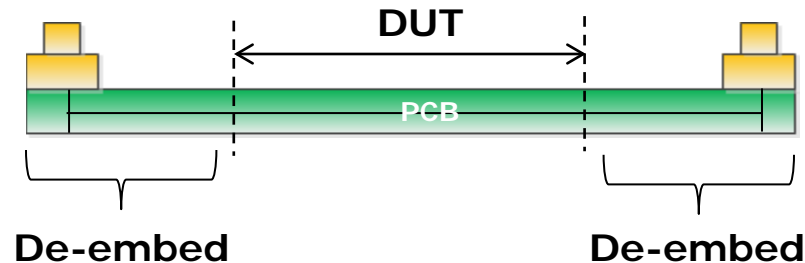
Example 5: PCB trace attenuation

ISD vs. eigenvalue (Delta-L)

- De-embed short trace (+ launch) from long trace (+ launch) to get trace-only attenuation.



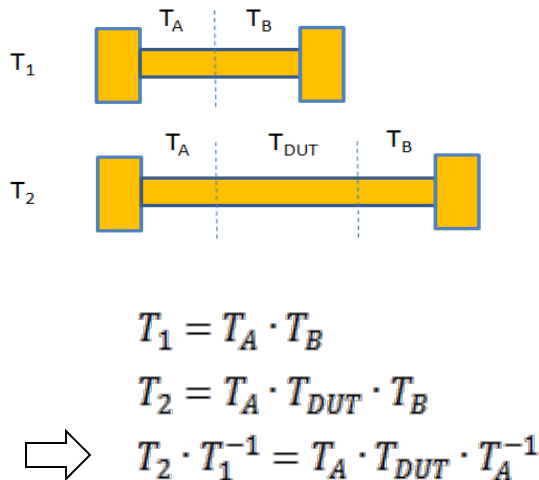
$$L_{\text{DUT}} = L_{\text{LONG}} - L_{\text{SHORT}}$$



Eigenvalue solution: not de-embedding

For calculating trace attenuation only

- Convert S to T for short and long trace structures
- Assume the left (and right) sides of short and long trace structures are identical
- Assume DUT is uniform transmission line
- Trace-only attenuation is written in one equation.



For uniform transmission line:

$$T_{DUT} = P \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} \cdot P^{-1}$$

Let $T_2 \cdot T_1^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}$

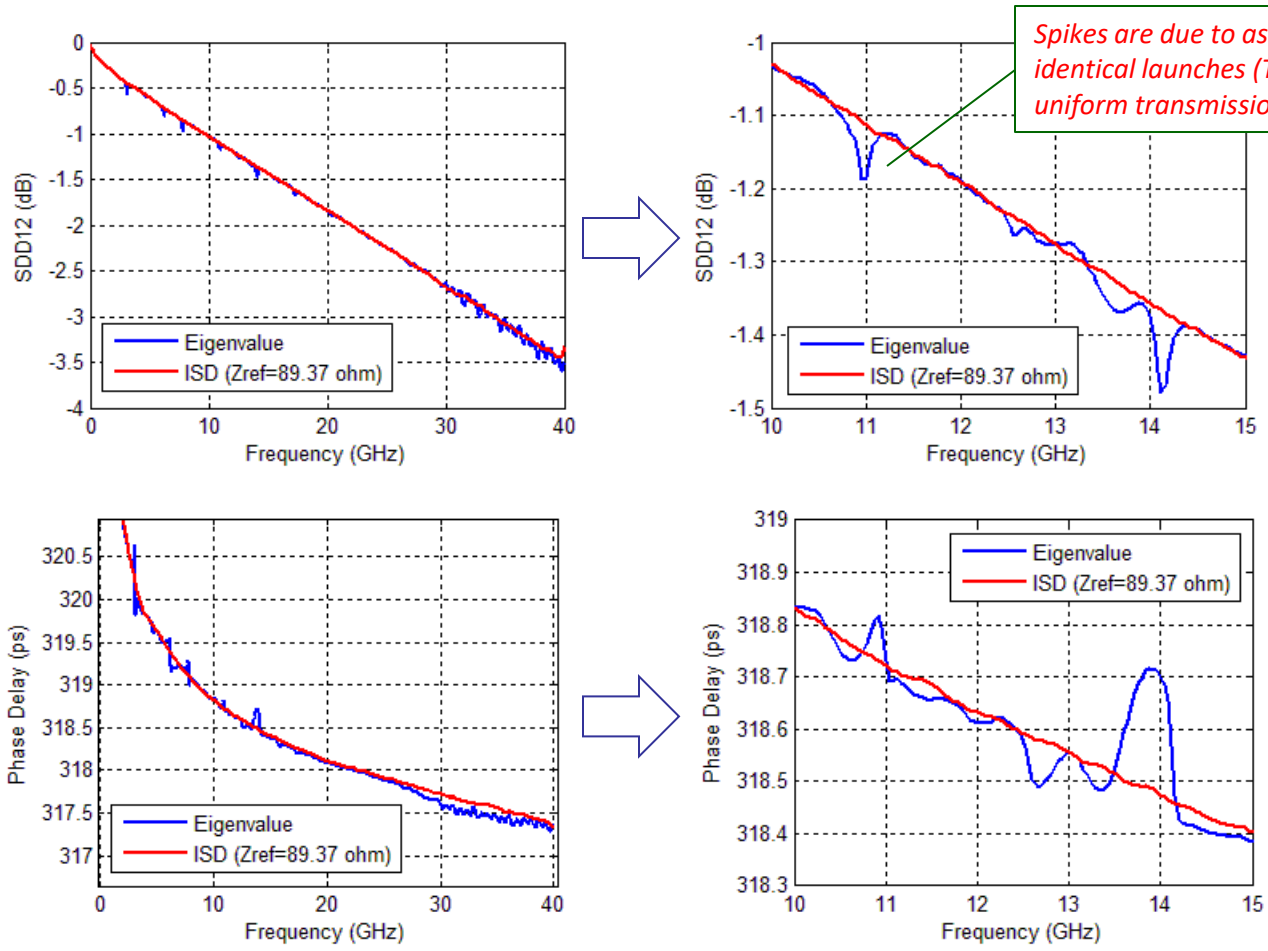
$\Rightarrow e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2}$

eigenvalue

modal propagation
constant

Case 1: 2" (=7"-5") trace attenuation

Eigenvalue solution is prone to spikes

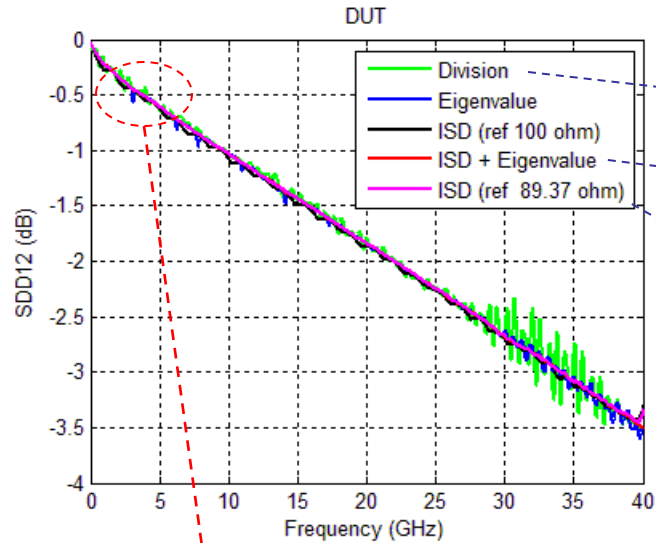


ISD's spike-free results help DK and DF extraction later.

One click compares ISD with eigenvalue and more...

Run	Help
Split 2x Thru only	
Extract DUT	
Batch mode	
Eigenvalue (Delta-L) method	
Compare ISD with Eigenvalue	
Renormalize and deskew DUT	
Material Property Extraction (MPX)	

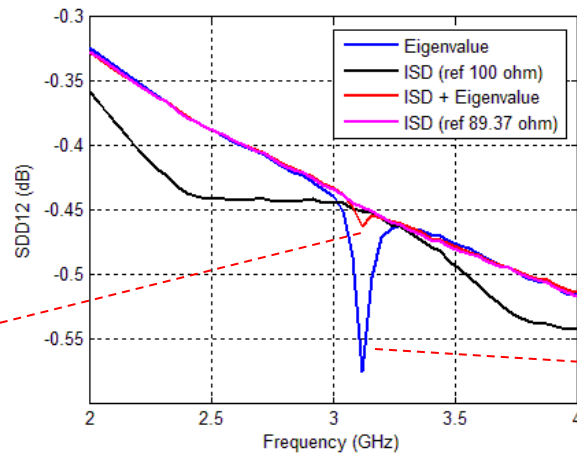
One click does it all



Direct dB subtraction

Eigenvalue of ISD results

Renormalize ISD results by trace impedance (automatically calculated)



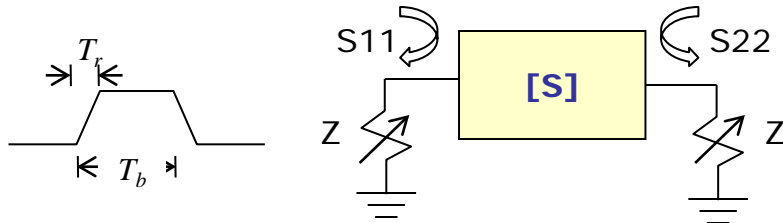
Spikes are due to assumption of uniform transmission line (T_{DUT}).

Spikes are due to assumptions of identical launches (T_A and T_B) and uniform transmission line (T_{DUT}).

How to define trace impedance

PCB trace is non-uniform transmission line

- Define impedance by minimal RL*

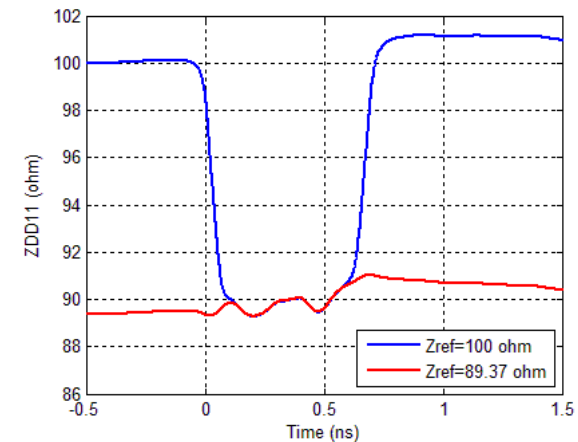
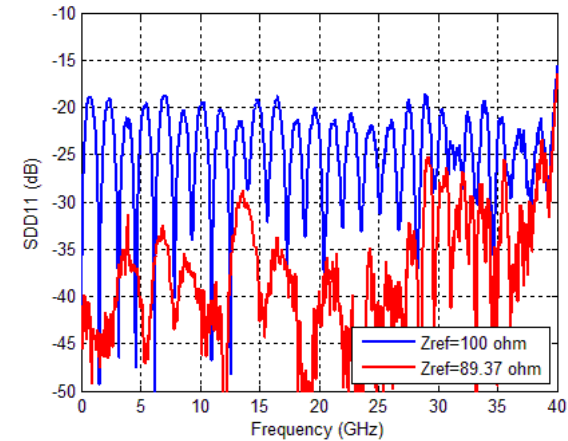
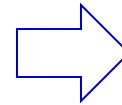


Minimize:

$$\varphi = \int_{f_{\min}}^{f_{\max}} \left\{ |S_{11}(f)|^2 + |S_{22}(f)|^2 \right\} \cdot |w(f)|^2 df$$

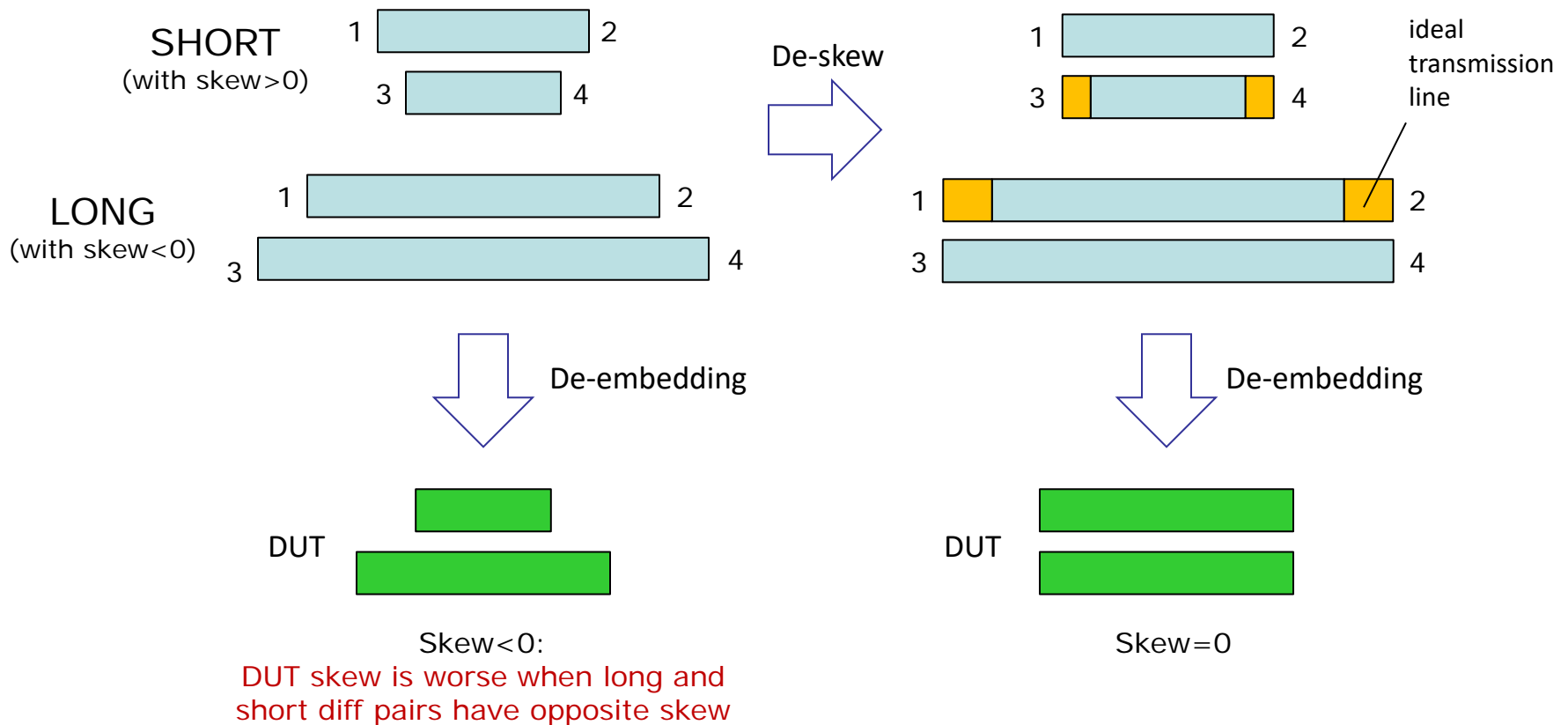
$$w(f) = \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}$$

* J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.

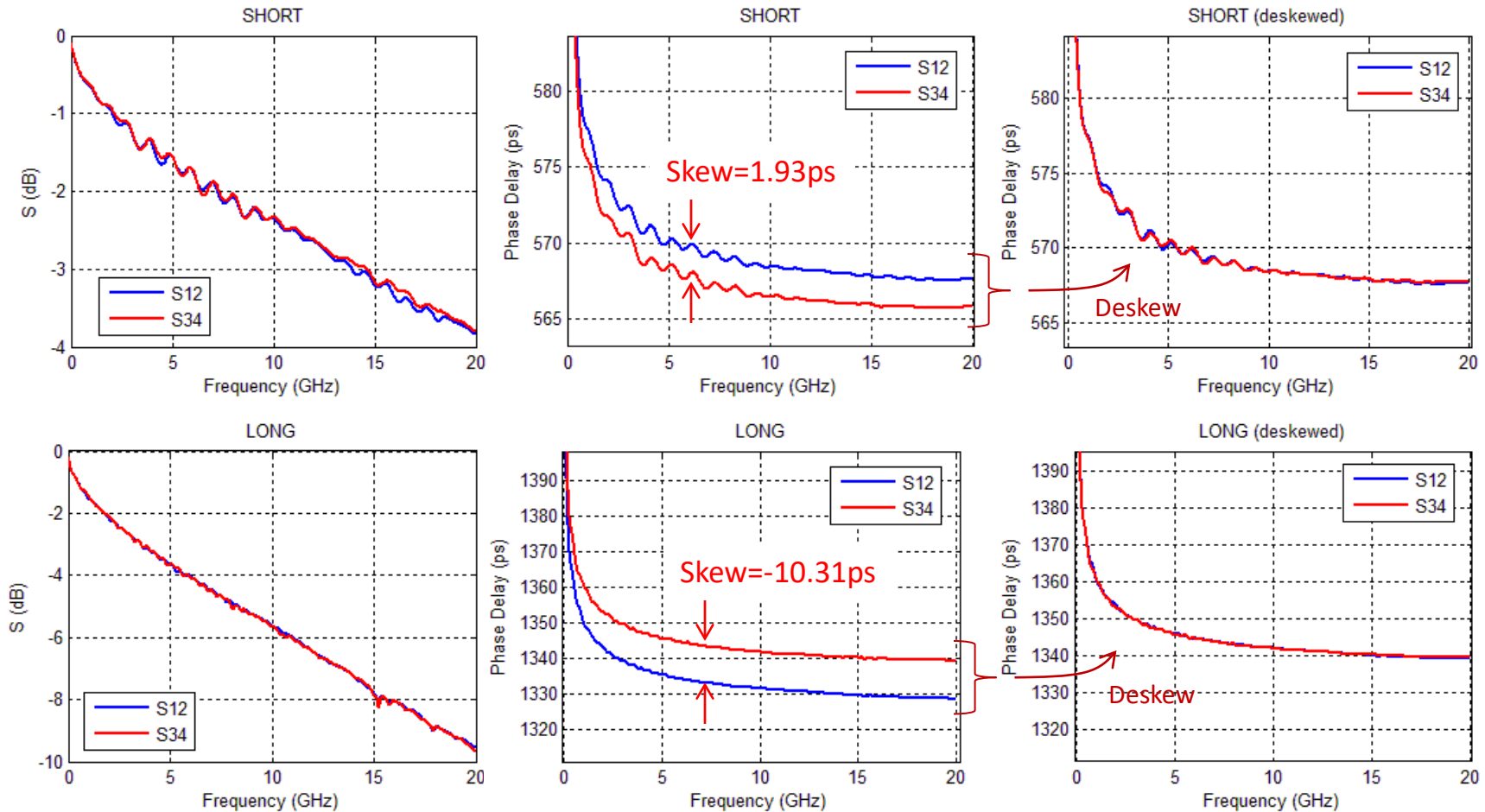


Skewless de-embedding

- Pad ideal transmission line to de-skew.

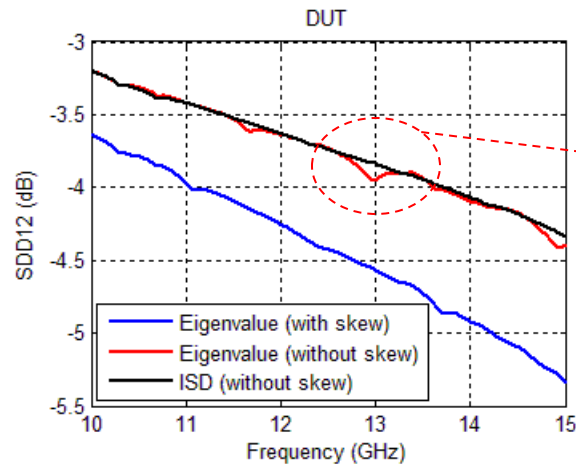
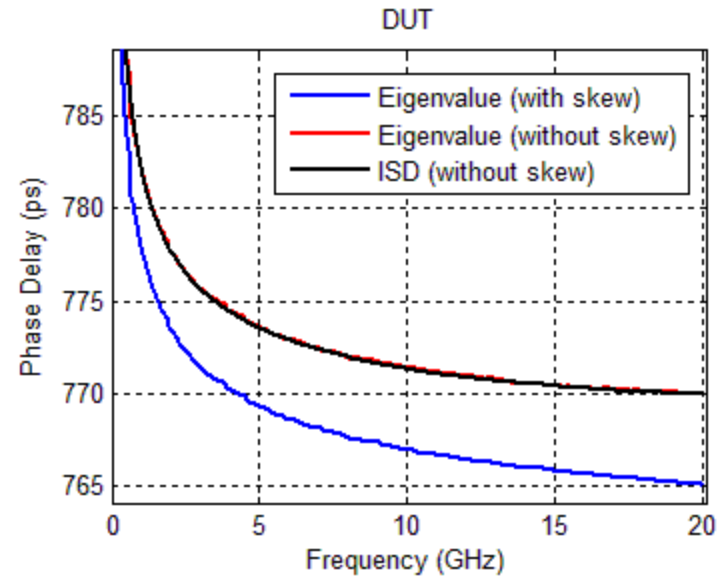
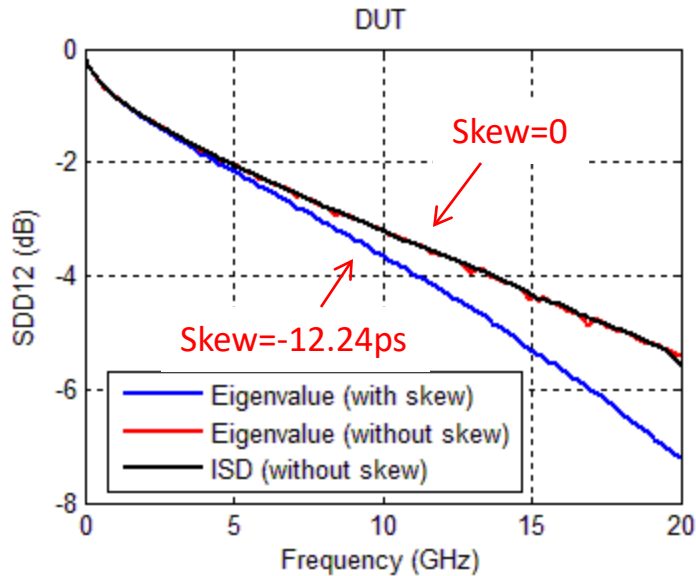


ISD optionally automates de-skewing of raw data



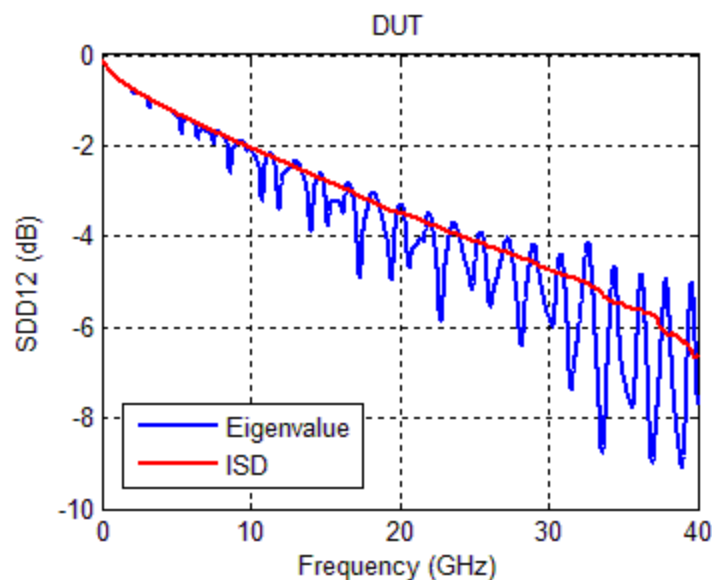
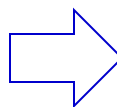
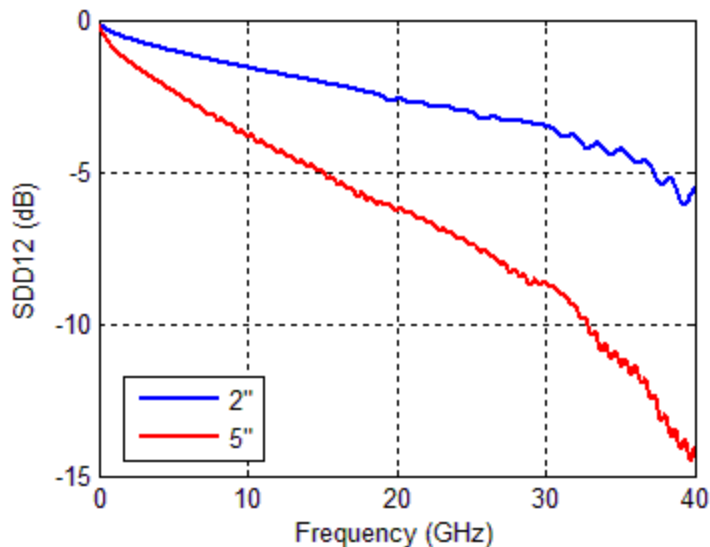
LONG=8"
SHORT=3"

Case 2: Extracted trace attenuation can be very different with or without skew



Eigenvalue solution has a dip at the frequency of interest (~12.9 GHz)

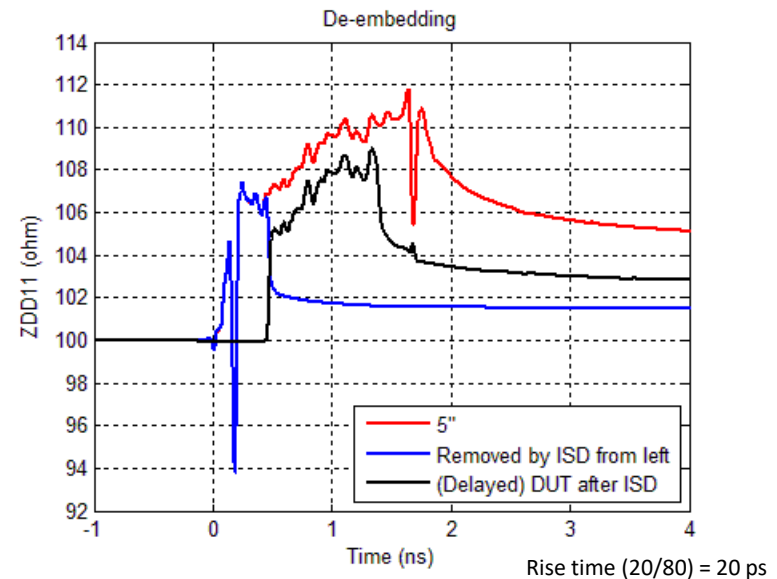
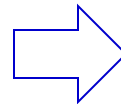
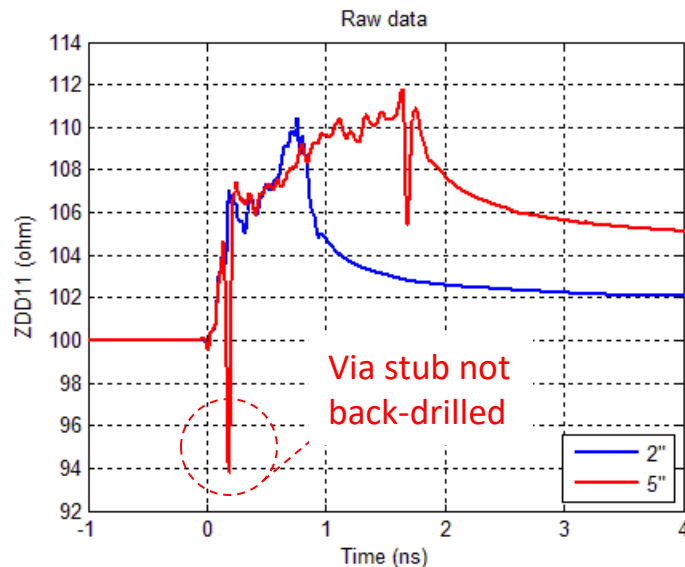
Case 3: Eigenvalue (Delta-L) solution becomes unstable in this case, but why?



TDR of raw data reveals why...

2" structure was back-drilled but 5" was not

- Eigenvalue solution assumes 2" and 5" structures have identical launches.
- ISD de-embeds 5" structure's launch correctly.

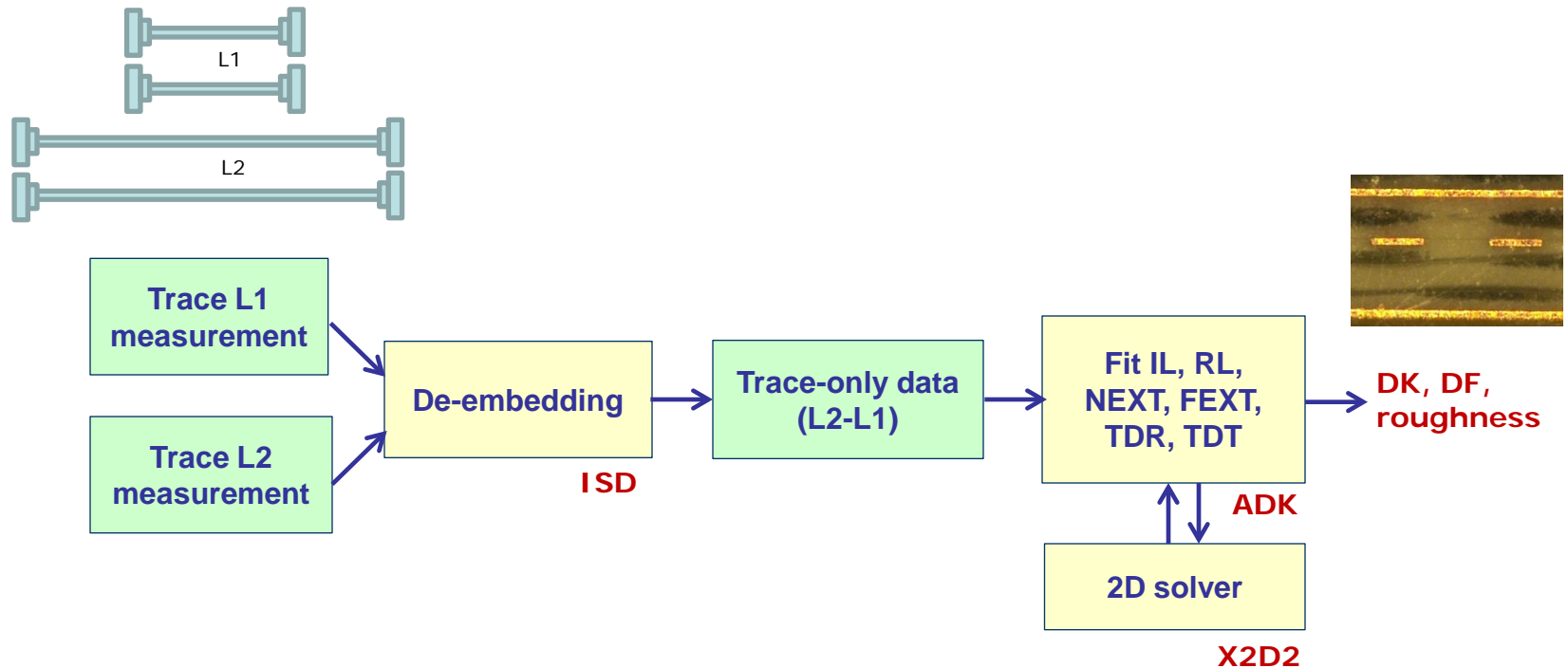


ISD saves \$\$\$ and time for not spinning another board.

Example 6: Material property extraction

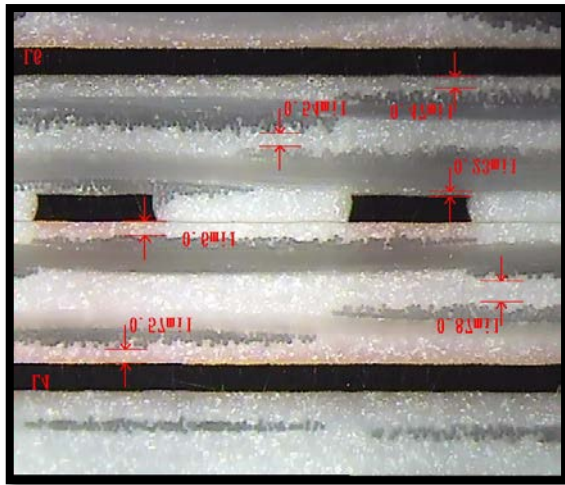
DK, DF and roughness

- Self consistent approach to extract DK, DF and roughness by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded trace-only data.

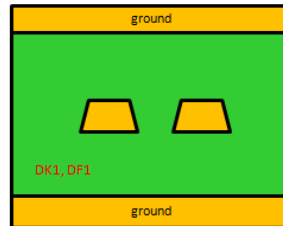


Automated extraction flow

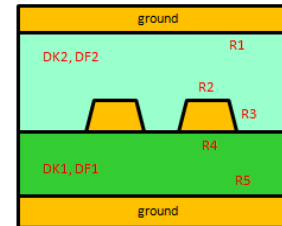
Models for cross section



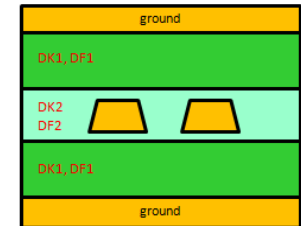
Optimized variables:
 DK1, DF1, DK2, DF2
 R1, R2, R3, R4, R5 (roughness)
 Metal width and spacing



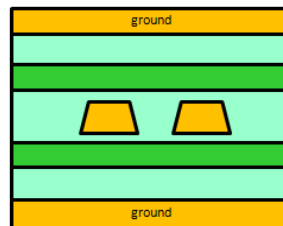
Model 1



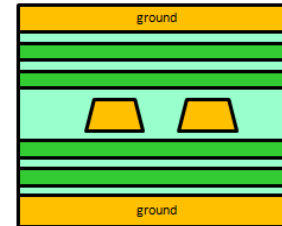
Model 2



Model 3



Model 4

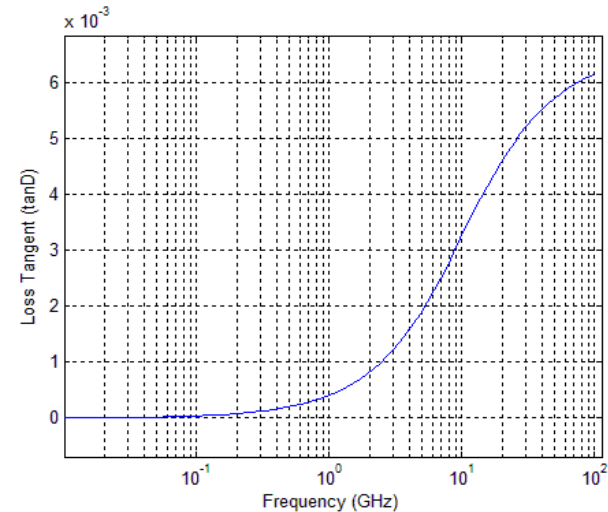
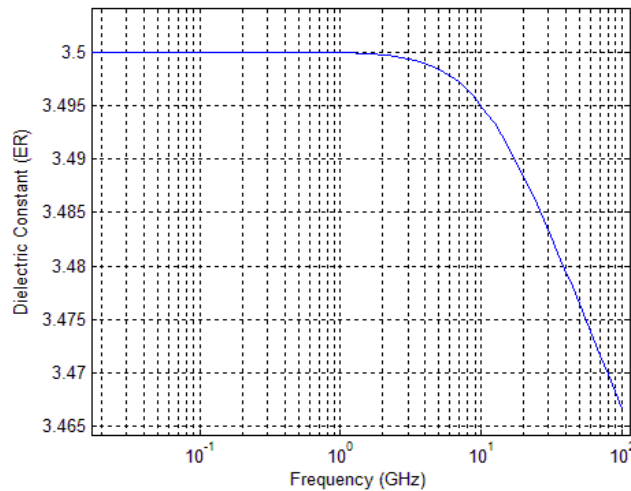


Model 5

Causal dielectric model

- Wideband Debye (or Djordjevic-Sarkar) model
 - Need only four variables: ε_∞ , $\Delta\varepsilon$, m_1 , m_2

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan \delta)$$



$$\varepsilon_\infty = 3.35 \text{ , } \Delta\varepsilon = 0.15 \text{ , } m_1 = 10 \text{ , } m_2 = 14.5$$

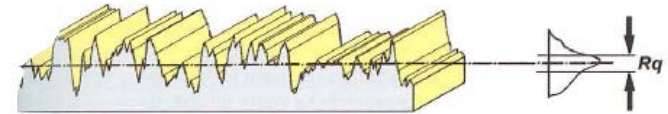
Surface roughness model

- Effective conductivity (by G. Gold & K. Helmreich at DesignCon 2014) needs only two variables: σ_{bulk} , R_q

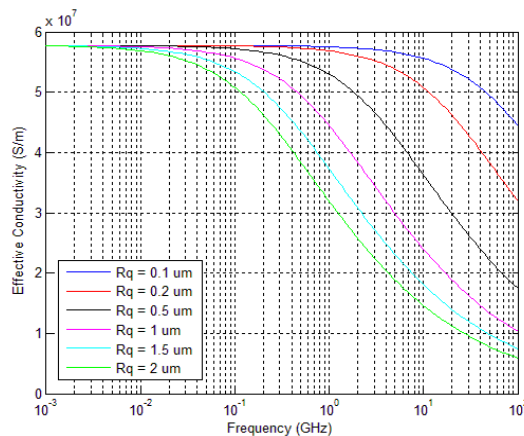
Parameter	Description	Standard
R_q	root mean square	DIN EN ISO 4287
R_a	arithmetic average	DIN EN ISO 4287, ANSI B 46.1
R_t	core roughness depth	DIN EN ISO 13565
R_z	average surface roughness	DIN EN ISO 4287

Table 1: Statistical parameters to describe surface roughness

$$\sigma(x) = \sigma_{bulk} \cdot CDF(x) = \sigma_{bulk} \cdot \int_{-\infty}^x PDF(x) du = \sigma_{bulk} \cdot \int_{-\infty}^x e^{-\frac{u^2}{2R_q^2}} du$$



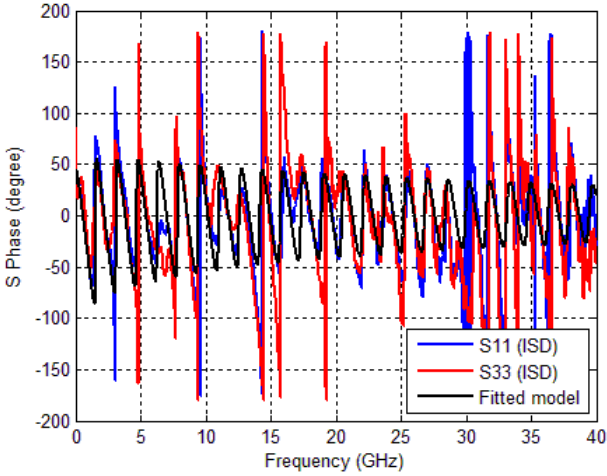
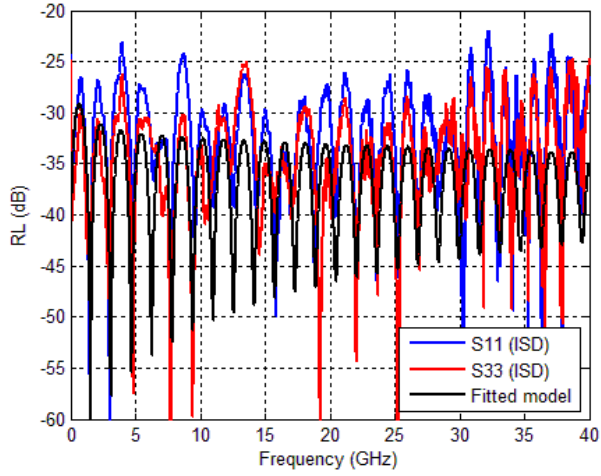
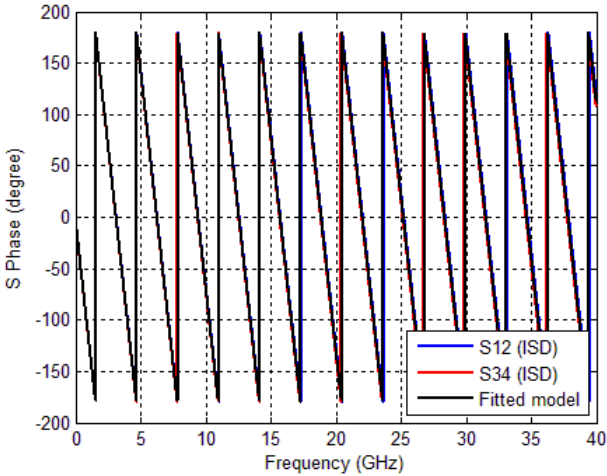
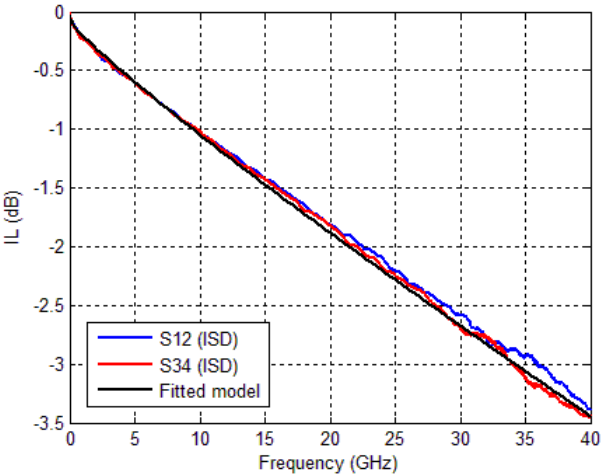
- Numerically solving $\nabla^2 \bar{B} - j\omega\mu\sigma\bar{B} + \frac{\nabla\sigma}{\sigma} \times (\nabla \times \bar{B}) = 0$ and equating power to that of smooth surface gives σ_{eff}



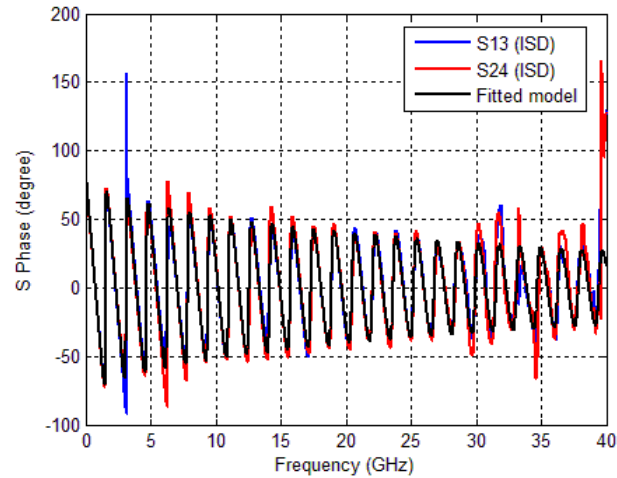
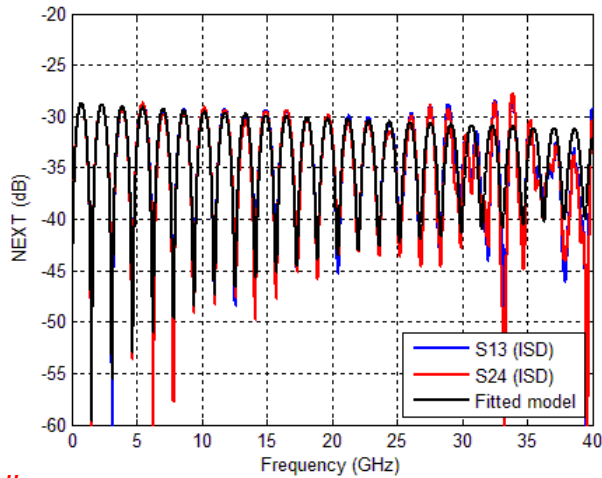
$$\sigma_{bulk} = 5.8 \times 10^7 \text{ s/m}$$

- ❖ Simple
- ❖ Work well with field solver
- ❖ Give effect of roughness on all IL, RL, NEXT and FEXT

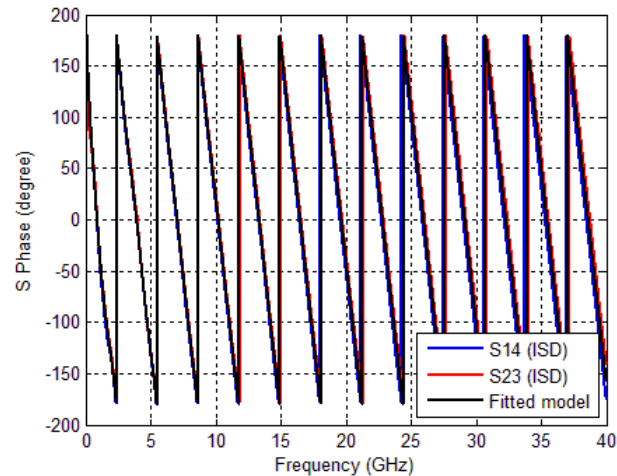
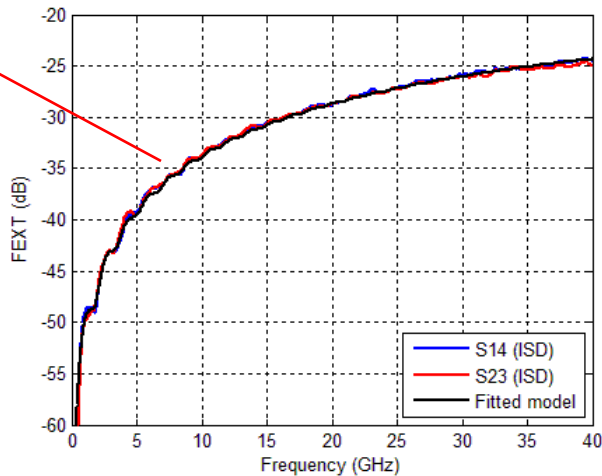
Matching IL and RL



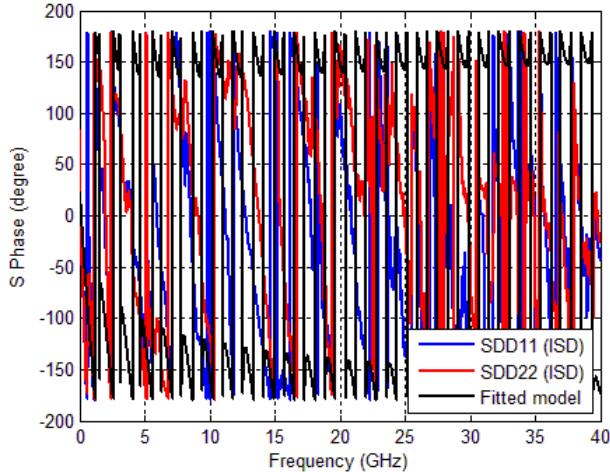
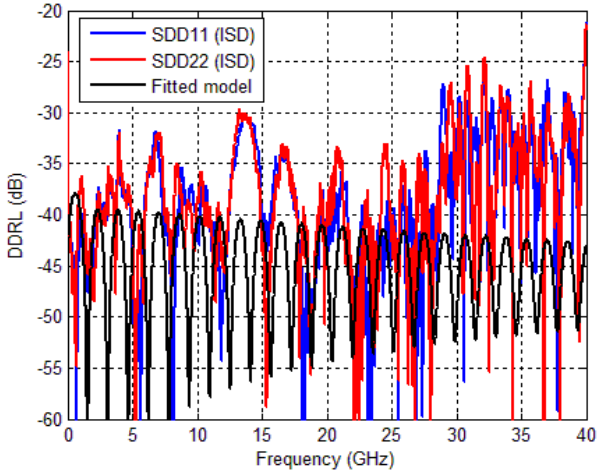
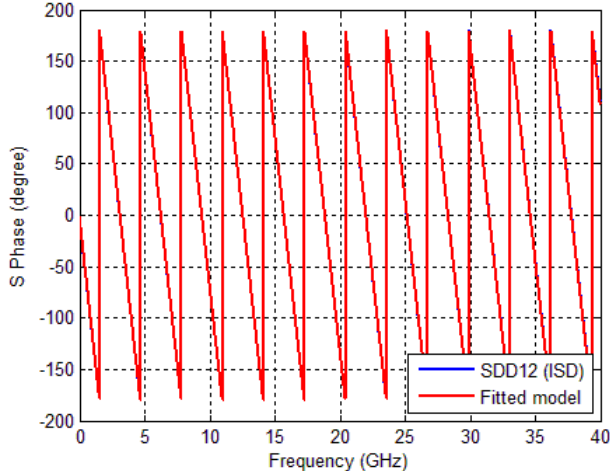
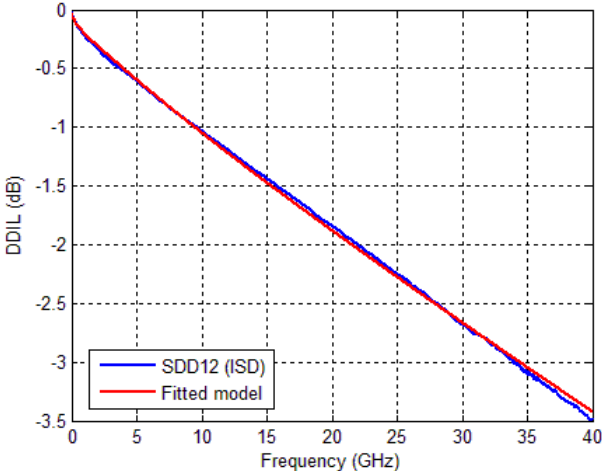
Matching NEXT and FEXT



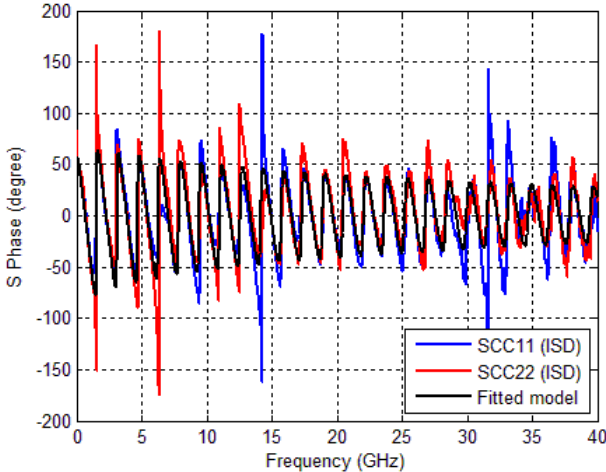
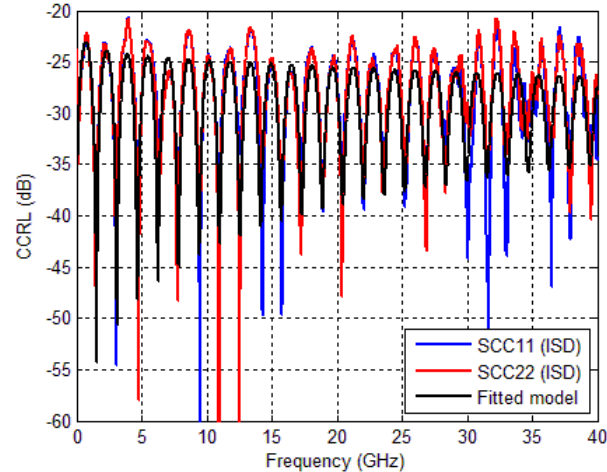
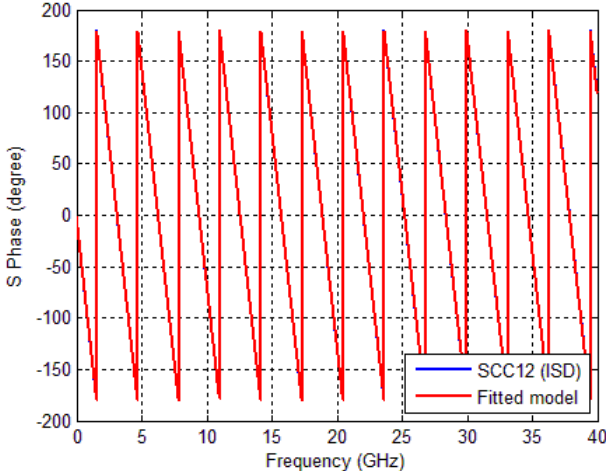
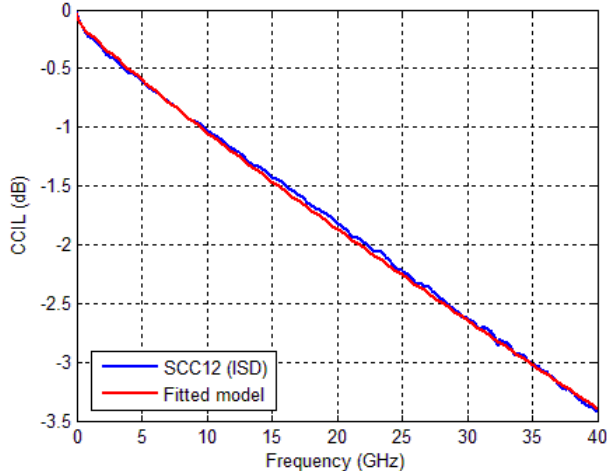
Large FEXT implies inhomogeneous dielectric



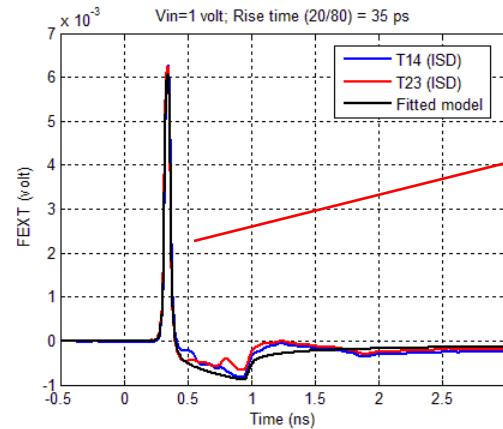
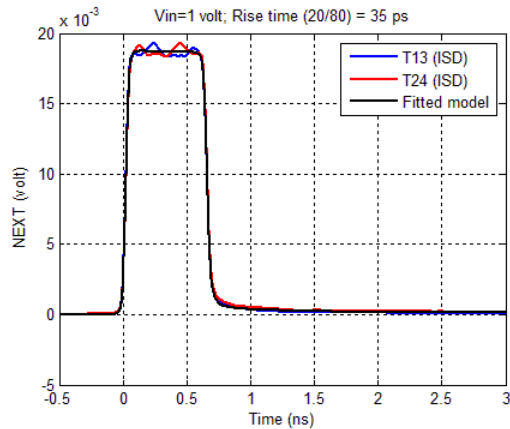
Matching DDIL and DDRL



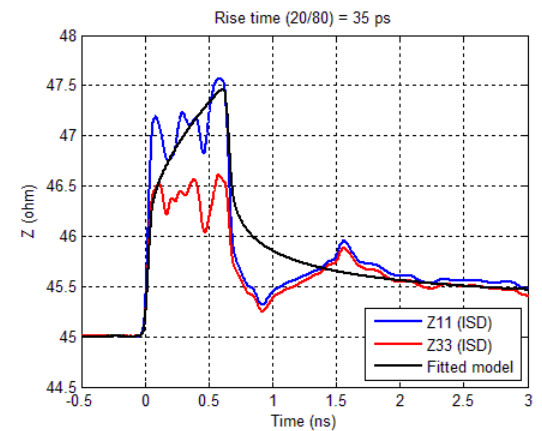
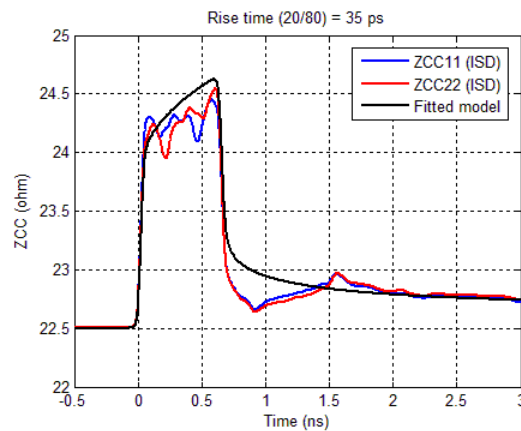
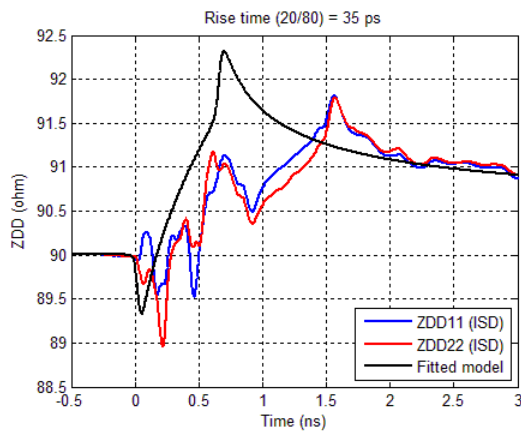
Matching CCIL and CCRL



Matching TDT and TDR

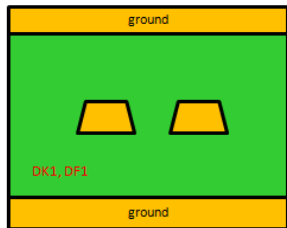


Positive polarity implies $K_C > K_L$

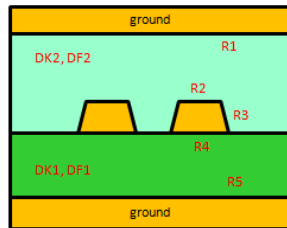


Comparison of Models 1 to 5

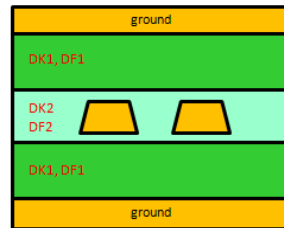
- Model 1 cannot match FEXT. Models 2 to 5 can match all IL, RL, NEXT, FEXT and TDR/TDT very well.



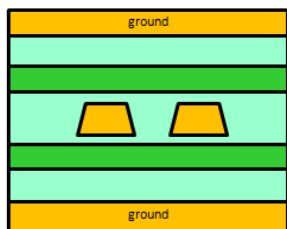
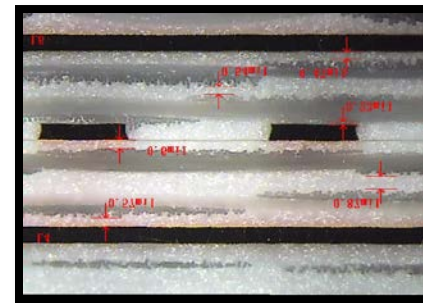
Model 1



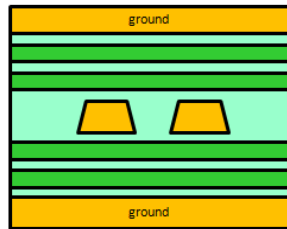
Model 2



Model 3



Model 4



Model 5

 DK1  DK2

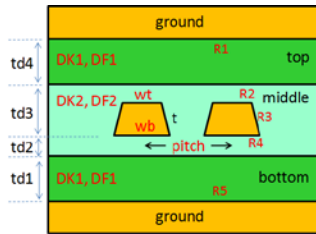
Model	DK1	DK2
1	3.510	-
2	2.444	4.294
3	3.413	3.623
4	3.863	3.360
5	3.115	3.975

At 10 GHz

DK2 > DK1 because of positive-polarity FEXT

Extracted DK1 and DF1

Model 3



$$\varepsilon_{\infty} = 3.27929$$

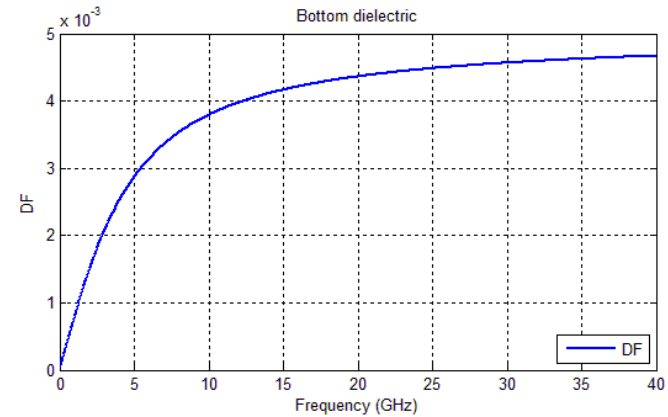
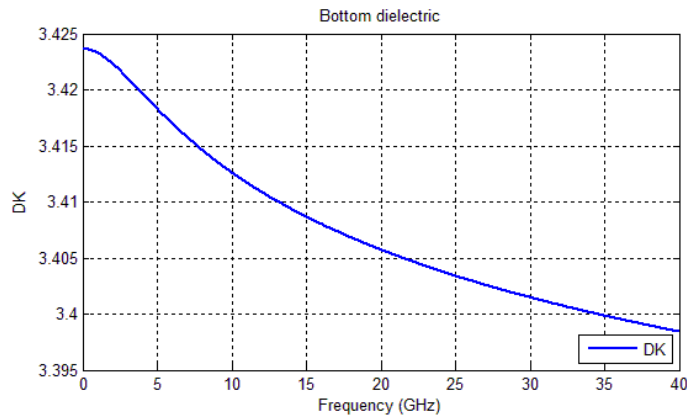
$$\Delta\varepsilon = 0.144348$$

$$m1 = 9.58619$$

$$m2 = 15.4109$$

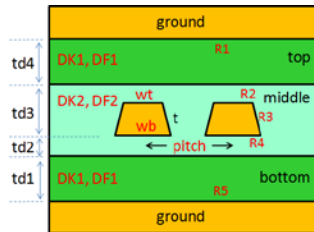
$$\varepsilon = \varepsilon_{\infty} + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right)$$

$$= \varepsilon_r \cdot (1 - i \cdot \tan \delta)$$



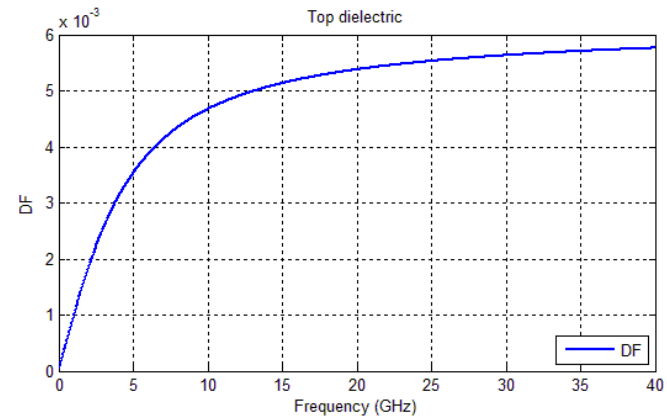
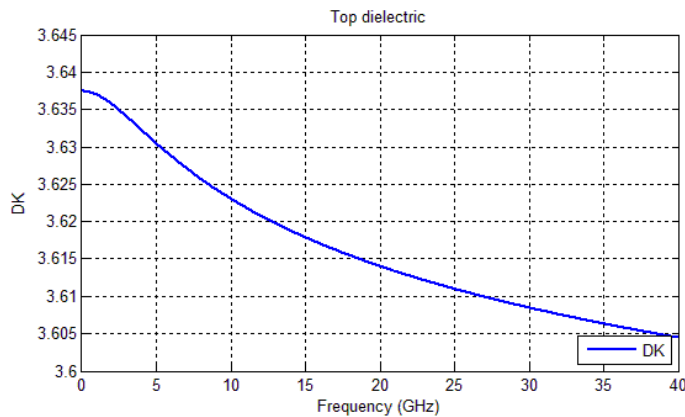
Extracted DK2 and DF2

Model 3



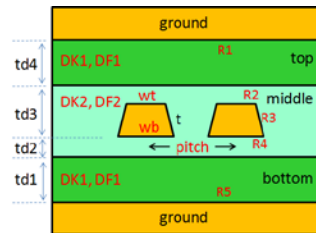
$$\begin{aligned}\varepsilon_{\infty} &= 3.46724 \\ \Delta\varepsilon &= 0.170196 \\ m1 &= 9.58715 \\ m2 &= 14.8352\end{aligned}$$

$$\begin{aligned}\varepsilon &= \varepsilon_{\infty} + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right) \\ &= \varepsilon_r \cdot (1 - i \cdot \tan \delta)\end{aligned}$$



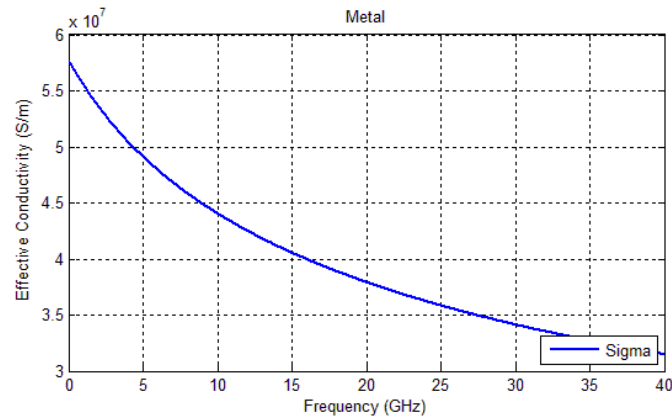
Extracted effective conductivity

Model 3

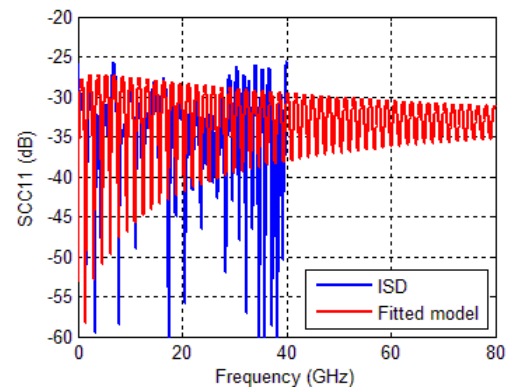
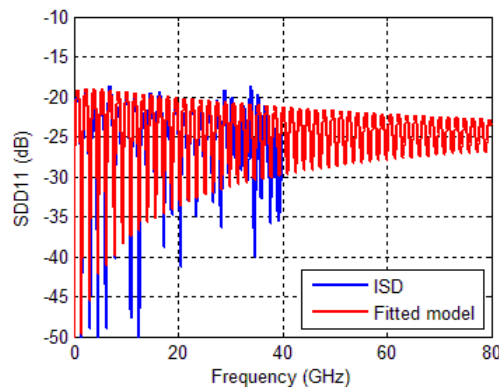
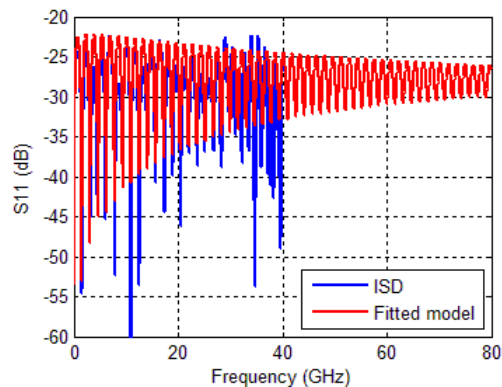
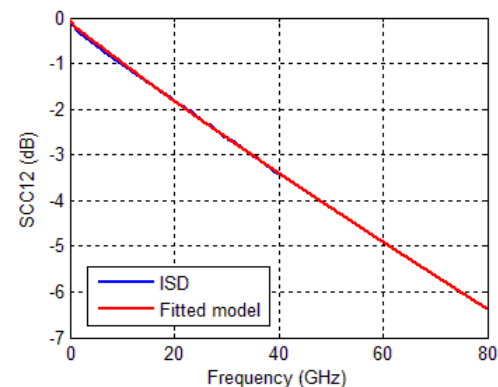
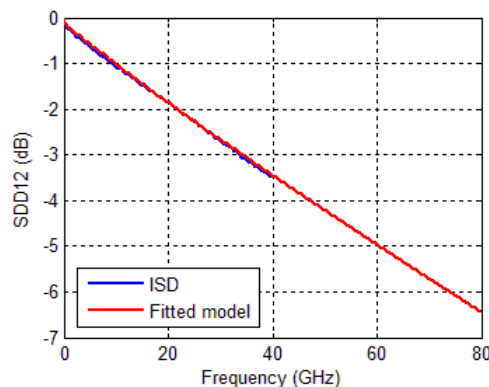
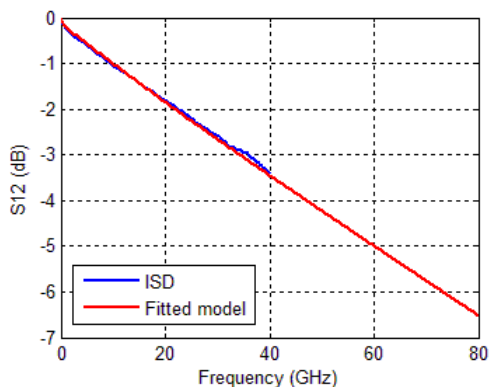


$$\sigma = 5.8 \times 10^7 \text{ S/m}$$

$$R_q = 0.324321 \mu\text{m}$$



Length- and frequency-scalable models can now be created.



Summary

- Accurate de-embedding is crucial for design verification, compliance testing and PCB material property (DK, DF, roughness) extraction.
- Traditional de-embedding methods can give non-causal errors in device-under-test (DUT) results if the test fixture and calibration structure have different impedances.
- In-Situ De-embedding (ISD) addresses such impedance differences through software instead of hardware, thereby improving de-embedding accuracy while reducing hardware costs.

Reference

- C.C. Huang, "Fixture de-embedding using calibration structures with open and short terminations," US patent no. 9,797,977, 10/24/2017.
- C.C. Huang, "In-Situ De-embedding," EDI CON, Beijing, China, 04/19 to 04/21/2016.
- C. Luk, J. Buan, T. Ohshida, P.J. Wang, Y. Oryu, C.C. Huang and N. Jarvis, "Hacking skew measurement," DesignCon 2018, 01/30 to 02/01/2018, Santa Clara, CA.
- H. Barnes, E. Bogatin, J. Moreria, J. Ellison, J. Nadolny, C.C. Huang, M. Tsiklauri, S.J. Moon, V. Herrmann, "A NIST traceable PCB kit for evaluating the accuracy of de-embedding algorithms and corresponding metrics," DesignCon 2018, 01/30 to 02/01/2018, Santa Clara, CA.
- J. Moreira, C.C. Huang and D. Lee, "DUT ATE test fixture S-parameters estimation using 1x-reflect methodology," BiTS China Workshop, 09/07/2017, Shanghai, China.
- J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.