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Reflectometry Techniques Aid IC Failure Analysis

Time-domain reflectometry can help you locate open and short failures in IC packages by comparing results with templates.

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Semiconductor manufacturers use time-domain reflectometry as a failure analysis (FA) tool because it can quickly perform nondestructive tests on packaged ICs. Time-domain reflectometry can isolate open and short-circuit defects in the three main regions of an IC: the die, the substrate, and the interconnects. The technique also works well with flip-chip (FC) and wire-bonded packages, and it can detect failures in packages mounted on PCBs.

At Texas Instruments, we now use time-domain reflectometry routinely in the lab to determine exactly where a signal pin is open or shorted and to measure the length of an electrical path. The discrepancies between the measured and expected characteristics of the electrical path help identify a fault location, or site.

In our tests, we use a digital sampling oscilloscope (DSO) equipped with a time-domain reflectometer (TDR) module. The TDR module generates a voltage edge with a fast risetime, and the DSO records that edge and the signals reflected back to the TDR. For simplicity, we'll call the combined instrument a TDR. **Figure 1** shows the waveform acquired with a probe connected to the TDR, but before connecting the probe to an integrated circuit or packaged device. The first voltage step in the waveform corresponds to the signal leaving the TDR, and the second step represents the reflection of the signal from the end of the probe tip. Because the first part of the TDR waveform provides no useful information, we shifted all our waveforms to start just before the time at which the signal reflects from the probe tip—the second step in Figure 1 (highlighted).

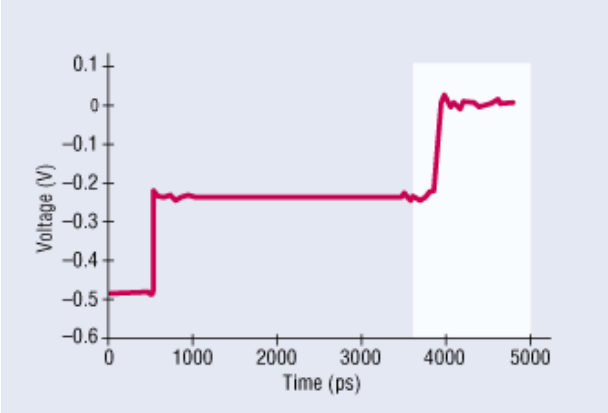

Figure 1. A TDR waveform includes the initial step of the TDR signal and the step reflected from the end of the probe tip (highlighted).

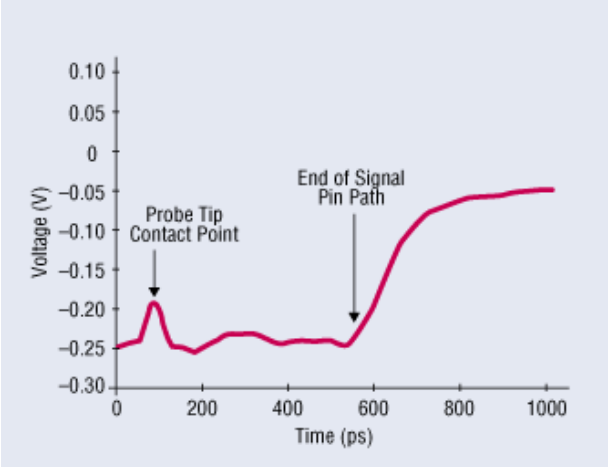

Figure 2. Typical TDR waveform from the signal pin on a packaged FC-BGA device shows the reflection from the probe

In our experience, devices undergoing testing need no special preparation, nor special fixturing. A pin on an IC or a via on a PCB serves as a convenient connection point. We placed DUTs on a flat, ESD-safe work surface and connected the probe tip to the signal pin of interest, and we connected the TDR's ground lead to the ground pin closest to the signal pin. Connecting to the closest ground pin reduces aberrations in the TDR waveform. You also could use a small thin sheet of metal about 2x2 in. square as a ground plane. Be sure to leave an opening for the signal pin to which you

want to connect. Then, connect the ground to the plane. This arrangement makes for easier connections because it eliminates the need for contacting a signal pin and a specific single ground connection. and the end of the device's signal path.

Figure 2 shows a TDR waveform measured at a signal pin on a packaged flip-chip BGA (FC-BGA) device. The connection of the probe tip to the device's signal pin reflects some of the test signal, but most of the signal reflects at the end of the signal path, located within the DUT. We were most interested in the time between when the signal was reflected from the probe tip and when it was reflected from the DUT. This period represents the total time it takes the signal to traverse through the DUT's transmission line and return to the probe. You can use this time to calculate the length of the electrical path along the transmission line. In Figure 2, the step for the signal pin's transmission path appears approximately 500 ps after the step at the probe tip.

Calculate Path Lengths

To calculate the length of the electrical path, multiply its velocity of propagation (VOP) by half the time measured between the probe-tip reflection and the reflection from the end of the DUT's transmission line. The TDR measured 230 ps between probe-tip and transmission-line end for an FC-BGA substrate (**Fig. 3**). The VOP value is 1.4×10^8 m/s for the FC-BGA substrate—copper traces embedded in FR-4 material.[1] We calculated a distance of 16.1 mm from the signal pin to the end of the electrical path, which agrees well with the actual 16.3 mm length of the substrate. This type of calculation will help you determine where a failure occurs in a package.

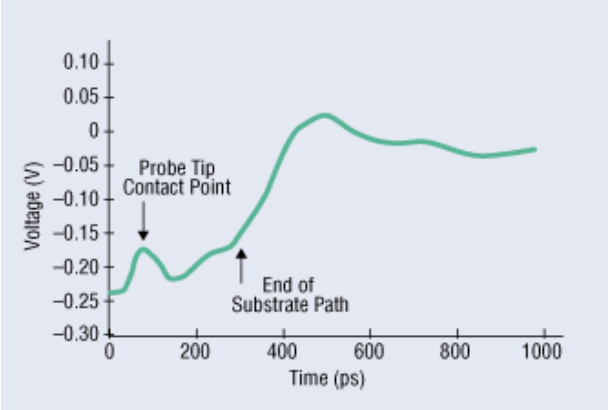

Figure 3. The TDR waveform from an unassembled substrate shows the effect of the short transmission line on the package.

You also can analyze failures by comparing the TDR waveform obtained from a failed device with waveforms from a known-good device and from an unassembled substrate. Comparing the three waveforms lets you quickly identify the main failure site.

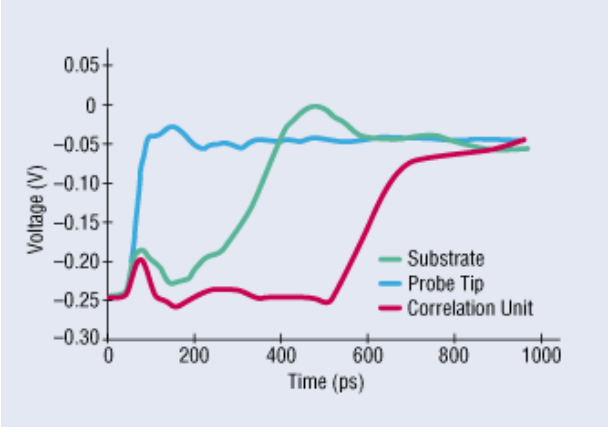

Figure 4. Superimposed TDR waveforms for the FC-BGA known-good unit, the unassembled substrate, and the probe tip show signals used for later comparison with waveforms from failed devices.

The graph in Figure 2 shows a typical TDR waveform for a signal pin on a known-good device in an FC-BGA package. Figure 3 shows the TDR waveform for the same signal pin on an unassembled substrate. Overlaying these two waveforms with the TDR waveform for the probe tip (highlighted portion of Fig. 1), as shown superimposed in **Figure 4**, identifies the limits for the three main failure-site regions: the substrate, the interconnect, and the die. The waveform obtained for the probe tip indicates the beginning of the electrical path. A DUT waveform that terminates to the left of the waveform for the substrate would indicate an open in the substrate. A DUT waveform that terminates just to the right of the substrate waveform would indicate an open in the interconnect region; one that ends tens of picoseconds to the right of the substrate waveform would indicate an open in the die.

The most challenging aspect of comparative TDR analysis involves distinguishing between a failure in the interconnect region and a failure in the die, because the distance between these regions can be as small as several microns. To help locate failures in this area, we recommend you build your own database of waveforms associated with each failure site in a specific type of device so you will have correlation waveforms for future analyses. Because these types of failures don't involve the substrate, you can destroy

the substrate to more closely examine a failure. You could use a destructive technique, such as cross sectioning or deprocessing, to visually verify the type of failure revealed by the TDR trace. (Deprocessing involves decapping a device, removing polyimide die coating, removing glass passivation, and so on.)

Comparative Analyses Locate Failures

To illustrate the TDR technique, we applied comparative analyses to three types of devices to locate failure sites within them. These device types included:

• three FC-BGA packages,

• a wire-bonded BGA package mounted in a standard socket, and

• a wire-bonded BGA device in a board assembly.

First, we analyzed three failed FC-BGA devices by obtaining TDR waveforms for the signal pin involved with the failure. For each device, we also obtained reference signal-pin TDR waveforms for a known-good device and for an unassembled substrate. We overlaid the signal-pin waveform of each failed device with the corresponding reference waveforms to produce a single graph.

The graph for the first device (**Fig. 5**) indicated an open on the substrate because the TDR trace occurs at a shorter time than for the substrate alone. We visually confirmed a crack in the signal-pin's trace line (**Fig. 6**), resulting from cracked laminate material. The TDR waveform for the second FC-BGA device (**Fig. 7**) showed an open in the interconnect region, as indicated by a reflection time between those for the substrate and for a correlation unit, or known-good unit, also confirmed visually (**Fig. 8**). Nonwetting of the solder bump on the die and the bump on the substrate caused this open. The third FC-BGA produced a TDR waveform that indicated an open in the die. We did not physically analyze the die to further isolate the cause of the open.

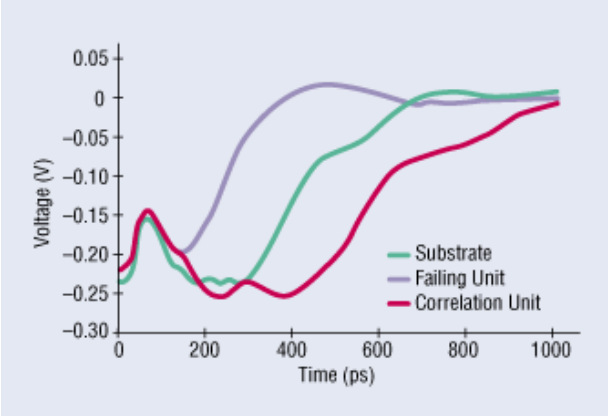

Figure 5. A TDR analysis of a failed FC-BGA unit indicates an open located in the substrate.

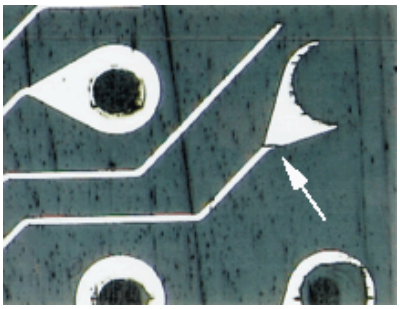

Figure 6. The image of the cracked trace line in the substrate shows the open associated with the waveform shown in Figure 5.

Second, we examined a failed wire-bonded BGA device to identify the site of short circuits. Analysis with a curve tracer indicated a short to ground for a signal pin in the fine-pitch device, but it couldn't show where in the package the short occurred. The distance, or pitch, between individual signal pins was approximately 0.5 mm, so we couldn't directly connect the probe tip and ground connection to the package leads. Instead, we used a standard socket.

Because we used a socket, we had to account for its effect on the TDR waveform from the DUT. So, we acquired a TDR waveform from the signal pin on the empty socket and then acquired the TDR waveform of a known-good device in the socket.

Finally, we put the DUT in the socket and acquired its waveform.

The waveform of the failed DUT showed a positive offset, a characteristic of a short circuit in a transmission line. We positioned the waveform of the failed device to overlap at the start with the other waveforms (**Fig. 9**). The overlapping portions, from 0 to 150 ps, correspond to the electrical path through the socket. At 150 ps, the waveform of the empty socket diverges from the other waveforms, indicating the start of the electrical path through the device. The waveforms of the failing unit and the known-good unit continue to overlap for another 250 ps. At about 400 ps, the waveforms from the DUT and the known-good device diverge. (The waveform for the known-good device increases.) This point of divergence corresponds to the point at which the short circuit occurs.

We didn't analyze the failed device any further. But an analysis of an identical short-circuit failure in a device from the same production lot revealed a metal bridge on an output transistor causing a short. The metal bridging was found after deprocessing the die, removing the metal-3 layer, and inspecting the die with a scanning electron microscope.

Third, we applied the TDR technique to test a wire-bond BGA device mounted on a PCB. We needed to determine whether a fault occurred on the board or in the BGA package. We first obtained the signal-pin waveform for an unassembled board and then for a known-good PCB assembly—a good PCB containing a good device. Finally, we acquired the TDR signal for the signal pin on the failed PCB assembly. The overlaid waveforms suggested an open within the device package, near or within the die.

Analyze Signatures, Too

We have also experimented using signature analysis to directly correlate the contours of the TDR waveform with each element in an FC-BGA's electrical path. The elements include the die, solder bump, substrate pad, and substrate trace line. First, we recorded the TDR waveform for a specific signal pin of a complete FC-BGA device. Then, we removed parts

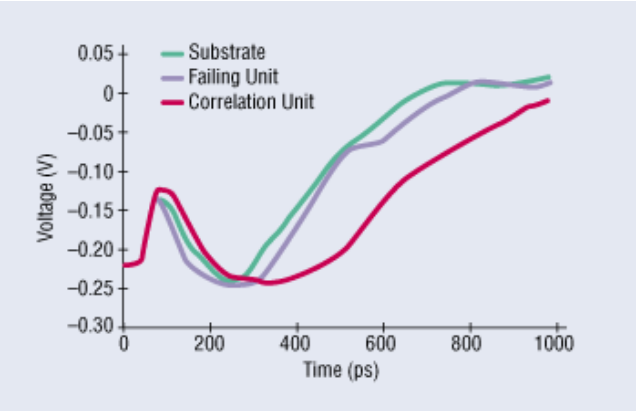

Figure 7. This set of TDR waveforms shows the failed unit's waveform closely approximates that of the substrate. This closeness indicates the open occurs in the interconnect region.

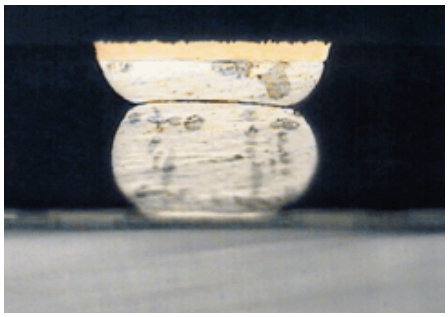

Figure 8. The open illustrated by the waveforms in Figure 7 arise from the nonwetting solder bumps shown here.

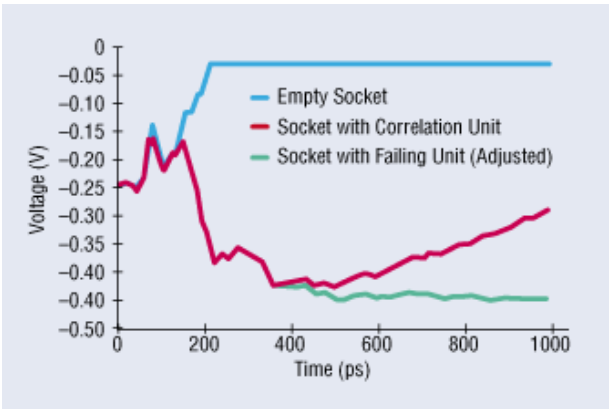

Figure 9. TDR waveforms for a socketed device show superimposed waveforms for the socket, the socket with a known-good device, and the socket with a failed device.

of the electrical path using backside parallel polishing and recorded TDR waveforms at each step (**Fig. 10**). The parts removed include the die, the bump array and substrate pads, and finally, the substrate trace line.

The waveforms shown in Figure 10 demonstrate that each element in the electrical path produces specific parts of the TDR waveform acquired for a complete package. You can locate a failure site by comparing the signal-pin waveform of a failed device with the "signature waveforms" obtained from a known-good device picked apart by the technique described above. The point at which the waveform of the failed device deviates from the signature waveform indicates the location of a fault.

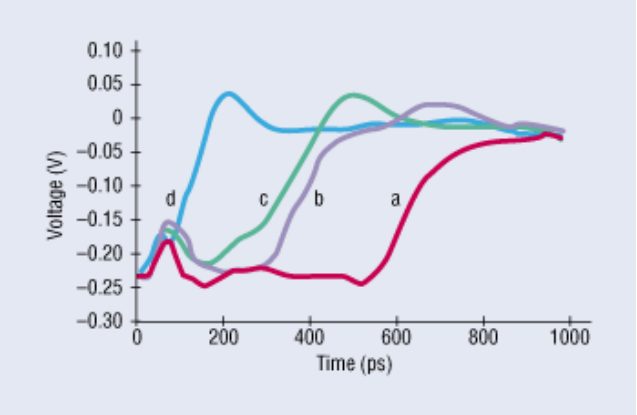

Figure 10. Superimposed waveforms show the results of measurements on a) a complete FC-BGA package, b) a package with die removed, c) a substrate with the solder-bump array and substrate pads removed, and d) a substrate with the trace lines removed.

In our experience, TDR techniques can provide useful information about failures in packaged devices. The lab setup is fairly simple, and it lets you produce meaningful results quickly. *T&MW*

FOOTNOTES

1. Blood, Bill, "MECL System Design Handbook," HB205, 4th ed., Motorola, Semiconductor Products Sector, Phoenix, AZ, 1988. p. 48.

FOR FURTHER READING

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