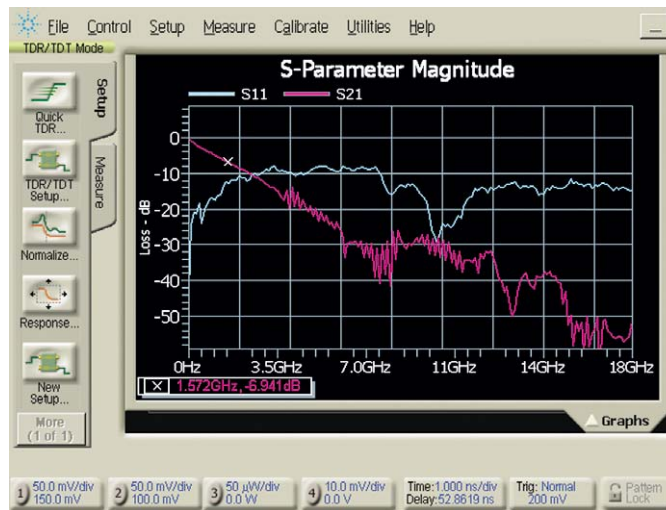


Agilent 86100C-202 S-Parameter and Time Domain Characterization

Complete Channel Verification – Done Simply

The demand for greater transfer of voice, data and video over networks and the increasing demand by users for higher productivity have dramatically increased the need for higher speed signals. These signals place a greater burden on the physical channel and have stimulated the need for differential channels in serial data transfers. New and existing industry standards such as PCI Express, Serial ATA, USB and IPC increasingly call for the use of S-parameters and impedance measurements to ensure system verification and interoperability.



Complete S-parameters – obtained quickly

Once the time domain is captured, the user can quickly request the S-parameters of the chosen channel using the Agilent 86100C-202 Enhanced Impedance and S-Parameter Software. The user selects up to four parameters to view and compare against design and verification limits. Troubleshooting between time and frequency domain is an easy one-button push.

TDR calibration and the Agilent N1024A TDR Calibration Kit further enhance the accuracy of the S-parameter measurements. The combination of these two capabilities provides one of the most accurate views of any TDR solution in the industry.

Multiple and subsequent discontinuities often diminish the reported size of later discontinuities. The Agilent 86100C-202 Enhanced Impedance and S-Parameter Software adds capability to accurately calculate the impedance value versus time or distance into the device being tested.

For even more comprehensive views of single-ended and differential S-parameters, the Agilent 86100C DCA-J Infiniium Digital Communications Analyzer and 54754A Differential TDR Module work seamlessly with Agilent's N1930A Physical Layer Test System Software (www.agilent.com/find/plts).

The information gathered from time and frequency domain can be easily exported to other applications in the Touchstone file format to use in circuit simulations and to further enhance designs.

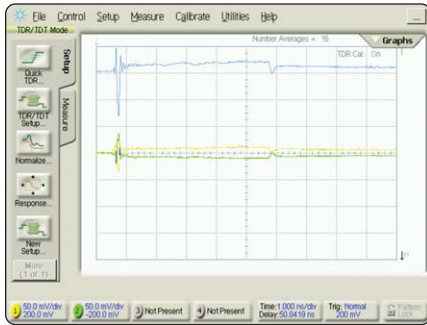
Differential or single-ended – characterized accurately

Many new communications systems use differential channels, which require additional R&D considerations and verification. Industry standards require designers and suppliers to characterize single-ended and differential parameters, encouraging designers to seek more streamlined and efficient methods.

Agilent provides the industry's cleanest time domain step, providing the most accurate view of time domain reflections and transmission. When performing verification of differential channels, the user is assured that they are seeing an accurate representation of the channel and where to best correct any design flaws or to troubleshoot during manufacturing.



Agilent Technologies



Simultaneously view single-ended and differential parameters.

The 86100C Infiniium DCA-J Digital Communications Analyzer, paired with the 54754A Differential TDR Module, quickly gives an accurate view of the delay and the impedance through the length of the device. The additional capability to see the minimum, maximum and average impedance of the channels helps the user verify to chosen limits.

Characterization of high speed channels

New high-speed channels often result in complex backplanes and printed circuit boards with 10 or more layers, very dense via fields and several connections. To maintain the signal integrity, the designer must know how the signals will interact with the

physical structures. For example, a clean, fast step may be required for characterization of small physical structures such as higher frequency connectors and smaller traces. The addition of Picosecond Pulse Lab's (www.picosecond.com) Source Enhancement Modules provides a quick and accurate view of closely-spaced discontinuities enabling the designer to select the appropriate circuit compensations.

For characterizing intermediate test points or channels without connectors, a wide range of single-ended and differential probes facilitate measurement closest to the point of interest.

Typical specifications

Step Rise Time: < 30 ps
 Step Flatness: +5/-3% up to 1 ns
 < 1% beyond 1 ns

Your choice to add these new capabilities to the 86100C mainframe and 54754A TDR module will protect your investment and allow you to upgrade existing assets. The combination of these solutions provides a very fast and cost-effective means to verify new designs and to speed your time to market.



Complete solution to view simultaneous return loss and insertion loss.

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